CPEG-323: Introduction to Computer Systems Engineering
Handout: Homework assignment 3
Issued: Monday, Oct. 6, 2008
Due Date: Wednesday, Oct. 15, 2008

Instructions

Please begin your answer to every problems on a new sheet of paper. Be as concise and clear as you can. Make an effort to be legible. To avoid misplacement of the various components of you assignment, make sure that all the sheets are stapled together. You may discuss problems with your classmates, but all solutions must be written up independently.

This homework will help you to advance your ability to apply knowledge in computer engineering learned in the course and Knowledge of related topics in computer science discipline.

Problem 1 (20 points)
Given the bit pattern:

\[
1011\ 1111\ 1110\ 0010\ 1010\ 0000\ 0111\ 0000
\]

What is the decimal value that this pattern represents, assuming that it is:

(a) An unsigned integer?

(b) A two’s complement integer?

(c) What is the BCD value if this bit pattern is an unsigned integer?

Problem 2 (20 points)
Do the Problem 3.31 in Patterson and Hennessy’s textbook(see page 232).

Problem 3 (20 points)
You have learned how to represent a negative number x in two’s complement representation(see slide 5 in Topic-3a). Please answer the following questions:

(a) state the rule of representing the negative number \(-x\) from x.
(b) prove the correctness of the principle.

**Problem 4 (20 points)**
You have learned how to fit a shorter number to a longer bits word in two’s complement representation (sign extension) (see slides 7-8 in Topic-3a). Please answer the following questions:

(a) Given two 4-bits signed numbers, represent them in 8-bits words.

\[
\begin{align*}
0111 \\
1011
\end{align*}
\]

(b) State the rule of sign extension.

(c) Prove the correctness of the principle.

**Problem 5 (20 points)**
On page 10 of the slides Topic3b, there is a figure that sketches the implementation of a 1-bit ALU. It can perform 1-bit operations such as "and", "or", "add", and "sub". The "XOR" gate in the figure is used to invert the value of "b". Suppose we chain 32 of this type of 1-bit ALUs with previous ALU’s CarryOut feed into the next ALU’s CarryIn. Therefore, we can perform WORD ALU operations on this 1-bit ALU array.

(a) For WORD "add" operation, the CarryIn signal in the least significant bit ALU is useless. But it is set to 1 for WORD "sub" operation. Please explain the reason.

(b) On page 15 of the slides Topic3b, we evaluate the delays needed for an N bit ripple adder. Now use the Carry Look-Ahead adder on page 21 of the slides Topic3b, analyze the gate delays of this adder compared to N = 32 ripple adder. For the Carry Look-Ahead unit, you can assume the delay to be 2 in canonical form.

(c) Finish the equations to build the Carry Look-Ahead unit from slide 22. Determine the maximum number of inputs required to make this a two-stage logic unit.