

CURRICULUM VITAE

NAME: Guang R. Gao

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EDUCATION

Ph.D Degree in *Electrical Engineering and Computer Science*
Massachusetts Institutes of Technology, August 1986.
Member of Computational Structures Group at Laboratory of Computer Science, MIT,
June 1982 to August 1986.

MS Degree in *Electrical Engineering and Computer Science*
Massachusetts Institutes of Technology, June 1982.

BS Degree in *Electrical Engineering*
Tsinghua University, Beijing.

PROFESSIONAL EXPERIENCE

University of Delaware

Newark, DE
Endowed Distinguished Professor, Department of Electrical and Computer Engineering, effective
from Sept. 1st, 2005

University of Delaware

Newark, DE
Professor, Department of Electrical and Computer Engineering, Sept. 1996 - Present
Founder and a leader of the Computer Architectures and Parallel Systems Laboratory (CAPSL).

McGill University

Montreal, Canada
Associate Professor, School of Computer Science, Jun. 1992 - Aug. 1999
Assistant Professor, School of Computer Science, Aug. 1987 - Jun. 1992
Founder and a leader of the Advanced Compilers, Architectures and Parallel Systems Group
(ACAPS) at McGill since 1988.

Center of Advanced Studies, IBM Toronto Lab

Aug. 1993 - Jun. 1994
Visiting scientist with a NSERC Senior Industrial Fellowship.

Philips Research Laboratories

Sept. 1986 - Jun. 1987
Briarcliff Manor, NY, US
Senior member of research staff of the Computer Architecture and Programming Systems Group.
Played a major role in founding a multiprocessor system project, and research in parallelizing
compilers.

Massachusetts Institutes of Technology

Jun. 1994 - Aug. 1994

Visiting Professor (Sabbatical)

Jun. 1980 - Aug. 1986

Member of the Computational Structures Group at the Laboratory of Computer Science, MIT. Participated in the MIT Static Dataflow Architecture Project and other projects.

Proposed a novel methodology of organizing array operations to exploit the fine-grain parallelism of dataflow computation models. Developed a unique pipelined code mapping scheme for dataflow machines (later known as dataflow software pipelining).

CURRENT RESEARCH AREAS:

Computer Architecture and Parallel Systems
Optimizing and Parallelizing Compilers

HONORS AND AWARDS

IEEE Fellow (class 2008)

ACM Fellow (2007)

PROFESSIONAL MEMBERSHIP

Member of ACM-SIGARCH, ACM-SIGPLAN

NATIONAL AND INTERNATIONAL RECOGNITION

IEEE Computer Society Distinguished Visitor, 1998 - 2001

Keynotes Speaker of Distinguished International Conferences

- 19th IEEE International Parallel and Distributed Processing Symposium 2005 (IPDPS 2005)
- 19th Annual International Symposium on High Performance Computing Systems and Applications (HPCS 2005)
- 2nd International Workshop on OpenMP 2006 (IWOMP 2006)
- 11th Asia-Pacific Computer Systems Architecture Conference (ACSAC 2006)
- IFIP International Conference on Network and Parallel Computing (NPC 2007)

International Advisory Board of EuroPar, 2000 - now

Recent honored special guest/invited professorship

- Tsinghua University, Beijing, China, Jun. 2007 - now
- Huazhong University of Science & Technology, China, Oct. 2004 - now
- Invited Professor for the Summer Schools of Numerical Analysis and Computer Science, France, Summer 2008

Invited speakers in universities, and R&D organizations in France, Germany, Holland, Sweden, England, Italy, Japan, China, Korea, and Taiwan.

PROGRAM COMMITTEE MEMBERS OF RECOGNIZED INTERNATIONAL CONFERENCES

ACM Computing Frontiers 2008

First Workshop on Programmability Issues for Multi-Core Computers (MULTIPROG 2008)

International Workshop on OpenMP (IWOMP'06, 08)

Eleventh Asia-Pacific Computer Systems Architecture Conference (ACSAC'06, 07, 08)

36th International Conference on Parallel Processing (ICPP'07)

ACM/IEEE International Conference for High Performance Computing and Communications (SC07)

ACM/IEEE 12th International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS 2007)

ACM International Conference on Supercomputing (ICS'95, 02, 03, 04, 06, 07)

IEEE International Parallel and Distributed Processing Symposium (IPDPS'01, 02, 03, 06)

5th IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES 2006)

IFIP International Conference on Network and Parallel Computing (NPC'04, 05, 06)

Fifth IEEE International Workshop on High Performance Computational Biology (HiCOMB'06)
ACM International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN 2005)
ACM/IEEE International Symposium on Micro architectures (MICRO'95, 96, 97, 02)
High Performance Computing Symposium (HPCS'95, 96, 98, 99, 01, 02).
International Conference on Parallel Processing (EURO-PAR'95, 96, 01)
IFIP and ACM SIGARCH International Conference on Parallel Architectures and Compilation Techniques (PACT'94, 95, 96, 97, 98, 99, 00, 01)
Compilers, Architectures and Synthesis for Embedded Systems (CASES'00, 01)
IEEE International Symposium on High Performance Computer (HPCA'97, 99, 00)
International Conference on Compiler Construction (CC'98, 99, 00), Europe.
Working Conference on Massively Parallel Programming Models (MPPM'93, 95, 97, 99)
International Symposium on High Performance Computing (ISHPC'99), Japan.
ACM Symposium on Programming Language Design and Implementation (PLDI'98)
International Parallel Processing Symposium (IPPS'95)
IEEE International Conference on Algorithms and Architectures for Parallel Processing (ICAPP'95)
Parallel Architecture and Language Europe (PARLE'91, 92, 93, 94, 95)

CONFERENCE COMMITTEE CHAIRMANSHIP

Vice Program Chairman of the 36th International Conference on Parallel Processing (ICPP'07)
Program Chairman of International Workshop on OpenMP (IWOMP'2007)
General Chair of International Conference on Embedded and Ubiquitous Computing (EUC'04)
Program Co-Chair of IFIP International Conference on Network and Parallel Computing (NPC'04)
Program Vice-Chair of IEEE International Parallel & Distributed Processing Symposium (IPDPS'04)
Program Vice-Chair of IEEE/ACM International Conference on High Performance Computing (HiPC'01)
Program Co-Chair of the Compilers, Architectures and Synthesis for Embedded Systems (CASES'01)
Chair of the Third Workshop on Petaflop Computing, Feb. 1999. Annapolis, MD.
Co-Chair of the Multithreaded Architecture Workshop, in Conjunction to HPCA'99, Orlando, Florida, Jan. 1999.
General Co-Chair of ACM International Conference on Parallel Architectures and Compilation Techniques (PACT'98), Oct. 1998, Paris, France., co-sponsored by IFIP and IEEE Computer Society
Co-Chair of the Compiler and Architecture Support for Embedded Systems (CASES'98, 99), Washington D.C.
Program Chairman of ACM International Conference on parallel Architectures and Compilation Techniques (PACT'94), Aug. 1994, Montreal, Canada.

JOURNAL EDITORSHIP

Editorial Board of Journal of Chinese Computer Research and Development (2005 - 2009)
Parallel Processing Letters (2001 - now)
Editorial Board of IEEE Transactions on Computers (1998 - 2001)
Editorial Board of IEEE Concurrency Journal (1997 - 2000)
Editorial Board of the Journal on Programming Languages in Jan. 1996, and subsequently became one of the two Co-Editors of the journal (1997 - 1998)
Editorial Board of the International Journal of High Performance Computing and Networking (2003 - now)
Editorial Board of the Journal of Embedded Computing (2004 - now)
Guest Editor for the Special Issue on IEEE Transaction on Computers, Journal of Parallel and Distributed Computing, etc.

INVITED SEMINARS AND DISTINGUISHED SEMINARS (Partial)

Given seminars in many industrial and academic organizations:

IBM T.J. Watson Research Center
IBM Toronto Lab,
AT&T Bell Laboratories
BNR
HP Labs
SGI

DEC
U.S. Naval Research Laboratory
Massachusetts Institute of Technology
Stanford University
University of California, Berkeley
New York University
Cornell University
University of Maryland
University of Alberta
University of Colorado
University of Southern California
University of Toronto
University of Victoria
DOE Oak Ridge National Laboratory
DOE Saudi Arabia Lab
NASA Ames Research Center

Section A: Teaching and Research Supervision

For detailed information about this section, please refer to <http://www.capsl.udel.edu/>

Section B: Scholarship

B.1: RESEARCH INTERESTS AND ACCOMPLISHMENTS

The research work of G. R. Gao spans the areas of parallel computer architecture and compiler technology with emphasis on their application in high-performance parallel computing systems. His research contributions in these general areas are many, however, he is well known for significant contributions in the following topics spread within the two areas:

1. **Computer Architecture:** there are a number of topics Gao has made important contributions that have great impact in the field. To name a few: (1) multithreaded architecture models and features leading/ pioneered the conception and design of a unique fine-grain multithreaded architecture based on static dataflow models - the well-known EARTH (Efficient Architecture for Running THreads) model; EARTH has applied the principles of dataflow computation principles to parallel computer architectures built from commodity components while demonstrating a migration path from commodity to custom hardware technology for scalable performance – the lasting impact of which will be appreciated even more when the emerging technology revolution of multi-core chips will need to deal with similar issues on fine-grain parallelism that EARTH has addressed in the past; (2) a novel memory consistency model (i.e. the Location Consistency) -- a new memory model for shared memory machines that allows the implementation of an efficient cache coherence protocol which avoids invalidation traffic and requires neither bus snooping, nor directories; (3) novel architecture features exploring instruction-level parallelism (e.g. superscalar architecture support of short-lived variables, the fundamental notion of instruction-level parallelism smoothability and others), and support of dataflow-like synchronization [see his ACM ISCA-2007 paper (<http://www.capsl.udel.edu/pub/doc/papers/ISCA2007.pdf>)].

2. **Compiler Technology:** there are a number of topics Gao has made important contributions that have great impact in this field. To name a few: program analysis techniques (e.g. fast algorithms to compute and apply SSA form, loop nests optimization (e.g. collective loop fusion and optimization) and instruction scheduling and register allocation (e.g. register allocation based on interval graphs), and software pipelining. Software pipelining is one of the most important compiler technologies for the exploitation of instruction-level parallelism in code optimization for modern microprocessor architectures. Gao's contribution to software pipelining area is very impressive. Gao's work is unique as he has proposed to viewed the software pipelining problem from the angle of a dataflow program graph model that has led interesting and distinct paths to formulate and solve some of the hard problems facing software pipelining. For example, his work on inner-most loop software pipelining pioneered a novel integer linear programming based methodology to solve the scheduling and register allocation problems in software pipelining, and his most recent work by extending software pipelining for nested loops [see his ACM PACT 2007 paper ([not online yet](#)), ACM PLDI2005 paper (<ftp://ftp.capsl.udel.edu/pub/doc/papers/SSP-RegAlloc.pdf>), and IEEE/ACM CGO 2004 papers

(<ftp://ftp.capsl.udel.edu/pub/doc/papers/SSP-Scheduling.pdf>, <ftp://ftp.capsl.udel.edu/pub/doc/papers/SSP-CodeGen.pdf>)] have opened a new path to exploit parallelism for nested loops.

A quick Google search (scholar.google.com, with search criteria = author:"gr gao") can easily reveal over 200 journal and conference publications and over 2,000 citations for his publications in the related areas. Gao's work has attracted the attention of many researchers in diverse application areas. The influence of his work is apparent through the impact of his work in his areas and several modifications and extensions from of the approaches and algorithms pioneered by his work.

Gao's technical accomplishment are best represented by a number of equally well known and widely cited publications with distinct contributions and impact in the two main areas listed above. Below, we pick 3 top cited papers in these two areas (NOTE: each area may have several topics).

1. "A Design Study of the EARTH multiprocessor", Proceedings of the IFIP WG 10.3 Working Conference on Parallel Architectures and Compilation Techniques, PACT '95, pages 59-68, Limassol, Cyprus, ACM Press, June 1995. (This paper is the first publication of a now well known multithreading architecture model - namely the EARTH (Efficient Architecture for Running Threads) model and project where Gao is the PI. EARTH brings the benefits of dataflow computation principles to parallel computers built from commodity components. EARTH described in this article is unique in that it has demonstrated a gradual migration from commodity to custom hardware for fine-grain multithreaded architectures, pioneered the few active dataflow based architecture projects during this period of time (from mid 1990s) while most dataflow projected in the world have terminated in early 90s. With the emerging multi-core chip technology revolution the impact of this paper will be ever increasing.)
2. "Software Pipelining Showdown: Optimal vs. Heuristic Methods in a Production Compiler", Proceedings of the ACM SIGPLAN '96 Conference on Programming Language Design and Implementation, Pages: 1-11, Philadelphia, Pennsylvania, May 1996. (This paper introduced a new framework for software pipelining that formulates the resource constrained optimal software pipelining problem as an integer linear programming problem, and present both qualitative and quantitative comparison to the heuristic method used in industrial production compilers at that time. Software pipelining continued to be one of the most effective code optimization techniques for modern compilers, and this paper pioneered a new direction that has triggered a number of important follow up work both in Gao's own group and elsewhere.)
3. "Location Consistency -- A New Memory Model and Cache Consistency Protocol", IEEE Transactions on Computers, Vol. 49, No. 8, Pages: 798-813, August 2000. (This paper introduced location consistency, a new memory model for shared memory machines that does not rely on "memory coherence" and it allows the implementation of an efficient cache coherence protocol which avoids non-productive invalidation traffic and requires neither bus snooping, nor directories [11]. The contribution of this paper is fundamental as it opened up a very distinct path to look at the whole issue of memory consistency – it will have a lasting impact for the years to come.)

B.2: LIST OF RESEARCH PUBLICATIONS

The contributions are listed under the following category:

Referred Journal Publications
Referred Conference Publications
Books/ Book Chapters/ Notes Sets
Patents

A. Referred Journal Publications

1. Hongbo Rong, Zhizhong Tang, R.Govindarajan, and Alban Douillet, Guang R. Gao, Single-dimension software pipelining for multi-dimensional loops. ACM Transactions on Architecture and Code Optimization, Vol.4, No.1, January, 2007.
2. Weirong Zhu, Yanwei Niu, and Guang R. Gao, Performance Portability on EARTH: A Case Study across Several Parallel Architectures, Cluster Computing, Volume 10, Number 2, Page 115-126, 2007.
3. Haiping Wu, Ziang Hu, Joseph Manzano and Guang. R. Gao, Madd Operation Aware Redundancy Elimination, International Journal of Software Engineering and Knowledge Engineering, Vol. 15, No. 2, Pages: 357-362, 2005

4. Hongbo~Yang, R. Govindarajan, Guang R. Gao, ZiangHu, Improving Power Efficiency with Compiler-Assisted Cache Replacement, *Journal of Embedded Computing*, Vol. 1, No. 4, Pages: 487-499, 2005.
5. Robel Kahsay, Li Liao , Guang Gao, An Improved Hidden Markov Model for Transmembrane Protein Topology Prediction and Its Applications to Complete Genomes, *Bioinformatics*, Volume 21, Number 9, Pages: 1853-158, 2005.
6. Robel Kahsay, Guoli Wang, Guang Gao, Li Liao and Roland Dunbrack, Quasi-Consensus Based COMParison of Profile Hidden Markov Models for Protein Sequences, *Bioinformatics*, Volume 21, Number 10, Pages: 2287-2293, 2005
7. Weirong Zhu, Yanwei Niu, Jizhu Lu, Chuan Shen and Guang R. Gao, A Cluster-Based Solution for High Performance Hmmpfam Using EARTH Execution Model, *International Journal of High Performance Computing and Networking*, Vol 2, Issue 2/3/4, 2004.
8. Parimala Thulasiraman, Kevin B. Theobald, Ashfaq A. Khokhar, and Guang R. Gao, Efficient Multithreaded Algorithms for the Fast Fourier Transform, *Parallel and Distributed Computing Practices*, Vol. 5, No. 2, Pages: 177-191, 2004.
9. Parimala Thulasiraman, Ashfaq A. Khokhar, Gerd Heber, Guang R. Gao, A Fine-Grain Load Adaptive Algorithm of the 2D Discrete Wavelet Transform for Multithreaded Architectures, *Journal of Parallel and Distributed Computing (JPDC)*, Vol.64, No.1, Pages: 68-78, January 2004.
10. Dong Rui Fan, Hongbo Yang, Gaung R. Gao, and Rong Cai Zhao, Evaluation and Choice of Various Branch Predictors for Low-Power Embedded Processor, *Journal of Computer Science and Technology*, Vol. 18, No. 6, Pages: 833-838, November, 2003.
11. Guy Tremblay, Christopher J. Morrone, José N. Amaral, and Guang R.Gao, Implementation of the EARTH Programming Model on SMP Clusters: a Multi-Threaded Language and Runtime System, *Concurrency and Computation: Practice and Experience*, Vol. 15, No. 9, Pages: 821-844, August 2003.
12. Ramaswamy Govindarajan, Hongbo Yang, José N Amaral, Chihong Zhang, and Guang R. Gao, Minimum Register Instruction Sequencing to Reduce Register Spills in Out-of-Order Issue Superscalar Architectures, in *IEEE Transactions on Computers*, Vol. 52, No. 1, Pages: 4-20, January 2003.
13. Ramaswamy Govindarajan and Guang R. Gao, Minimizing Buffer Requirements in Rate-Optimal Schedules in Regular Dataflow Networks, *Journal of VLSI Signal Processing*, Vol. 31, No. 3, Pages: 207-229, Jul 2002.
14. Adalberto T. Castelo, Wellington S. Martins, and Guang R. Gao, TROLL--Tandem Repeat Occurrence Locator, *Bioinformatics*, Vol. 18, No. 4, Pages: 634-636, April 2002.
15. Ramaswamy Govindarajan, Erik R. Altman, and Guang R. Gao, A Theory for Co-Scheduling Hardware and Software Pipelines in ASIPs and Embedded Processors, *Design Automation for Embedded Systems*, Vol. 6, No. 3, Pages: 243-275, March 2002.
16. Robel Y. Kahsay, Nataraj Dongre, Guang R. Gao, Guoli Wang, and Roland L. Dunbrack Jr., CASA: A Server for The Critical Assessment of Sequence Alignment Accuracy, *Bioinformatics*, Vol. 18, No. 3, Pages: 496-497, March 2002.
17. José N Amaral, Wen-Yen Lin, Jean-Luc Gaudiot, and Guang R. Gao, Exploiting Locality in single Assignment Data Structures Updated through Split Phase Transactions, *Cluster Computing*, Special issue on Internet Scalability: Advances in Parallel, Distributed and Mobile Systems, Vol. 4, No. 4, Pages: 281-293, October 2001.
18. Prasad Kakulavarapu, Olivier Maquelin, José N Amaral, and Guang R. Gao, Dynamic Load Balancers for a Multithreaded Multiprocessor System, *Parallel Processing Letters*, Vol. 11, No. 1, Pages: 169-184, March 2001.
19. Guang R. Gao and Vivek Sarkar, Location Consistency-- A New Memory Model and Cache Consistency Protocol, *IEEE Transactions on Computers*, Vol. 49, No. 8, Pages: 798-813, August 2000.
20. Gerd Heber, Rupak Biswas, Guang R. Gao, Self-avoiding walks over adaptive unstructured grids, *Concurrency: Practice and Experience*, Vol. 12, Iss. 2-3, Pages: 85 - 109, Jun. 2000.
21. Xinan Tang and Guang R. Gao, Automatically Partitioning Threads for Multithreaded Architectures, *Special Issues on Compilation and Architectural Support for Parallel Applications*, *Journal of Parallel and Distributed Computing*, Vol. 58, No. 2, Pages: 159-189, August 1999.
22. Walid A. Najjar , Edward A Lee, and Guang R Gao, Advances in the Dataflow Computational Model, *Parallel Computing* , Vol. 25, No.13 - 14, Pages: 1907 – 1927, 1999.

23. Erik R. Altman and Guang R. Gao, Optimal Modulo Scheduling Through Enumeration, *International Journal on Parallel Programming*, Vol. 26, No.2, Pages: 313-344, 1998.
24. Erik R. Altman, Ramaswamy Govindarajan, and Guang R. Gao, A Unified Framework for Instruction Scheduling and Mapping for Function Units with Structural Hazards, *Journal of Parallel and Distributed Computing*, Vol. 49, No. 2, Pages: 259-293, 1998.
25. Vugranam C. Sreedhar, Guang R. Gao, and Yong-Fong Lee, A New Framework for Elimination Based Data Flow Analysis Using DJ Graphs, *ACM Transaction on Programming Languages and Systems*, Vol. 20, No. 2, Pages 388-435, March 1998.
26. Vugranam C. Sreedhar, Guang R. Gao, and Yong-fong Lee, Incremental Computation of Dominator Trees, *ACM Transactions on Programming Languages and Systems*, Vol. 19, No. 2, Pages: 239-252, March 1997.
27. Vugranam C. Sreedhar, Guang R. Gao, and Yongfong Lee, A Quadratic Time Algorithm for Computing Multiple Node Immediate Dominators, *Journal of Programming Languages*, 1996.
28. Vugranam C. Sreedhar, Guang R. Gao, and Yongfong Lee, Identifying Loops Using DJ Graphs, *ACM Transactions on Programming Languages and Systems*, Vol. 18, No. 6, Pages: 649 – 658, November 1996.
29. Ramaswamy Govindarajan, Erik R. Altman, and Guang R. Gao. A Framework for Resource-constrained Rate-optimal Software Pipelining, *IEEE Transactions on Parallel and Distributed Systems*, Vol. 7, No. 11, Pages: 1133-1149, November 1996.
30. Herbert H. J. Hum, Olivier Maquelin, Kevin B. Theobald, Xinmin Tian, Guang R. Gao, and Laurie J. Hendren, A Study of the EARTH-MANNA Multithreaded System, *International Journal of Parallel Programming*, Vol. 24, No. 4, Pages: 319-347, August 1996.
31. Eshrat Arjomandi, William O'Farrell, Ivan Kalas, Gita Koblents, Frank Ch. Eigler, and Guang. R. Gao, ABC++: Concurrency by Inheritance in C++, *IBM Systems Journal*, Vol. 34, No. 1, Pages: 120-137, 1995.
32. Vugranam C. Sreedhar and Guang R. Gao, A Linear Time Algorithm for Placing OE-nodes, *Journal of Programming Languages*, 1995. Accepted.
33. Vugranam C. Sreedhar and Guang R. Gao, Computing phi-nodes in Linear Time Using DJ Graphs, *Journal of Programming Languages*, Vol. 3, Pages: 191-213, April 1995.
34. Qi Ning, Vincent V. Dongen, and Guang R. Gao, Automatic Data and Computation Decomposition for Distributed Memory Machines, *Parallel Processing Letters*, Vol. 5, No. 4, Pages: 539-550, April 1995.
35. Ramaswamy Govindarajan and Guang R. Gao, Rate-optimal Schedule for Multi-rate DSP Computations, *Journal of VLSI Signal Processing*, Vol. 9, No.3, Pages: 211-232, April 1995.
36. Guoning Liao, Guang R. Gao, Vinod K. Agarwal, A dynamically scheduled parallel DSP architecture for stream flow programming, *Journal of Microcomputer Applications*, Vol. 17, Iss. 2 Pages: 171 - 196, April 1994
37. Laurie J. Hendren, Guang R. Gao, Erik R. Altman, and Chandrika Mukerji, A Register Allocation Framework Based on Hierarchical Cyclic Interval Graphs, *The Journal of Programming Languages*, Vol. 1, No. 3, Pages: 155-185, 1993.
38. Guang. R. Gao, An Efficient Hybrid Dataflow Architecture Model, *Journal of Parallel and Distributed Computing*, Vol. 19, No. 4, Pages: 293-307, December 1993.
39. Qi Ning and Guang R. Gao, Optimal Loop Storage Allocation for Argument-fetching Dataflow Machines, *International Journal of Parallel Programming*, Vol. 21, No. 6, Pages: 421-448, December 1992.
40. Herbert H. J. Hum, and Guang. R. Gao, A High-speed Memory Organization for Hybrid Dataflow/von Neumann Computing, *Future Generation Computer Systems*, Vol. 8, Pages: 287-301, 1992.
41. Guang. R. Gao, Herbert H. J. Hum, and Yue-Bong Wong, Toward Efficient Fine-grain Software Pipelining and the Limited Balancing Techniques, *International Journal of Mini and Microcomputers*, Vol. 13, No. 2, Pages: 57-68, 1991.
42. Guang R. Gao, Exploiting Fine-grain Parallelism on Dataflow Architectures, *Parallel Computing*, Vol. 13, No. 3, Pages: 309-320, March 1990.
43. Guang R. Gao, Algorithmic Aspects of Balancing Techniques for Pipelined Data Flow Code Generation, *Journal of Parallel and Distributed Computing*, Vol. 6, No. 1, Pages: 39-61, 1989.
44. Guang R. Gao, A stability classification method and its application to pipelined solution of linear recurrences, *Parallel Computing*, Vol. 4. No. 3, Pages: 305-321, June 1987.

45. Guang R. Gao, A Maximally Pipelined Tridiagonal Linear Equation Solver, *Journal of Parallel and Distributed Computing*, Vol. 3, No. 2, Pages: 215-235, 1986.
46. Jack B. Dennis, Guang R. Gao, Kenneth W. Todd, Modeling the Weather with a Data Flow Supercomputer. *IEEE Transactions on Computers* Vol. 33, No. 7, Pages: 592-603, July 1984.

B. Referred Conference Publications

1. Liping Xue, Long Chen, Ziang Hu, Guang R. Gao, Performance Tuning of the Fast Fourier Transform on a Multi-core Architecture, accepted at the First Workshop on Programmability Issues for Multi-Core Computers (MULTIPROG), Goteborg, Sweden, January 27, 2008.
2. Lurng-Kuo Liu, Fei Chen, Christos J. Georgiou and Guang R. Gao, Server I/O Acceleration Using an Embedded Multi-core Architecture, accepted at the Workshop on Application Specific Processors (WASP'07), Salzburg, Austria, October 4, 2007.
3. Yuan Zhang, Evelyn Duesterwald and Guang Gao, Concurrency Analysis for Shared Memory Programs with Textually Unaligned Barriers, *Proceedings of The 20th International Workshop on Languages and Compilers for Parallel Computing (LCPC 2007)*, Urbana, Illinois, October 11-13, 2007.
4. Alban Douillet and Guang R. Gao, Software-Pipelining on Multi-Core Architectures, *Proceedings of the 16th International Conference on Parallel Architectures and Compilation Techniques (PACT 2007)*, Brasov, Romania, September 15-19, 2007.
5. Weirong Zhu, Vugranam C. Sreedhar, Ziang Hu, and Guang R. Gao, Synchronization State Buffer: Supporting Efficient Fine-Grain Synchronization for Many-Core Architectures, the 34th International Symposium on Computer Architecture (ISCA 2007), Pages: 35 – 45, San Diego, CA, USA, June 9-13, 2007.
6. Guangming Tan, Ninghui Sun and Guangrong Gao, A Parallel Dynamic Programming Algorithm on a Multi-core Architecture, 19th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA 2007), Pages: 135 – 144, San Diego, CA, USA, June 9 - 11, 2007.
7. Yuan Zhang, Vugranam C. Sreedhar, Weirong Zhu, Vivek Sarkar, Guang R. Gao, Optimized lock assignment and allocation: a method for exploiting concurrency among critical sections, In the *Proceedings of the 12th ACM SIGPLAN symposium on Principles and practice of parallel programming (PPoPP 2007)*, Pages: 146 – 147, San Jose, California, USA, March 14 - 17, 2007.
8. Long Chen, Ziang Hu, Junmin Lin, and Guang R. Gao, Optimizing Fast Fourier Transform on a Multi-core Architecture, *Workshop on Performance Optimization for High-Level Languages and Libraries(POHLL'07)*, in conjunction with 21th International Parallel and Distributed Processing Symposium (IPDPS 2007), Page(s):1 – 8, Long Beach, CA, USA, March 2007.
9. Ge Gan, Ziang Hu, Juan Cuvillo, Guang R. Gao, Exploring a multithreaded methodology to implement a network communication protocol on the Cyclops-64 multithreaded architecture, *First Workshop on Multithreaded Architectures and Applications(MATTP'07)*, in conjunction with 21th International Parallel and Distributed Processing Symposium (IPDPS 2007), Page(s):1 – 8, Long Beach, CA, USA, March 2007.
10. Weirong Zhu, Ziang Hu, and Guang R. Gao, On the Role of Deterministic Fine-Grain Data Synchronization for Scientific Applications: A Revisit in the Emerging Many-Core Era, *First Workshop on Multithreaded Architectures and Applications(MATTP'07)*, in conjunction with 21th International Parallel and Distributed Processing Symposium (IPDPS 2007), Page(s):1 – 8, Long Beach, CA, USA, March 2007.
11. Haiping Wu, Eunjung Park, Mihailo Kaplarevic, Yingping Zhang, Murat Bolat, Xiaoming Li, Guang R. Gao, Automatic Program Segment Similarity Detection in Targeted Program Performance Improvement, *Workshop on Performance Optimization for High-Level Languages and Libraries(POHLL2007)*, in conjunction with 21th International Parallel and Distributed Processing Symposium (IPDPS 2007), Page(s):1 – 8, Long Beach, CA, USA, March 2007.
12. Daniel Orozco, Liping Xue, Murat Bolat, Xiaoming Li, Guang R. Gao, Experience of Optimizing FFT on Intel Core Architecture, *Workshop on Performance Optimization for High-Level Languages and Libraries(POHLL'07)*, in conjunction with 21th International Parallel and Distributed Processing Symposium (IPDPS 2007), Page(s):1 – 8, Long Beach, CA, USA, March 2007.
13. Weirong Zhu, Parimala Thulasiraman, Ruppa K. Thulasiram and Guang R. Gao, Exploring Financial Applications on Many-core-on-a-chip Architecture: A First Experiment, *Workshop on Frontiers of High Performance Computing and Networking (FHPCN2006)*, in *Proceedings of 4th*

- International Symposium on Parallel and Distributed Processing and Applications (ISPA-06) , Sorrento, Italy, Dec.4-7, 2006; (Lecture Notes in Computer Science, Vol. 4331, pp.221-230, 2006).
14. Alban Douillet, Hongbo Rong, Guang R. Gao, Multidimensional Kernel Generation for Loop Nest Software Pipelining, In the Proceedings of Europar'2006, Dresden, Germany, August-September 2006.
 15. Ziang Hu, Juan del Cuillo, Weirong Zhu, Guang R. Gao, Optimization of Dense Matrix Multiplication on IBM Cyclops-64: Challenges and Experiences, In the Proceedings of Europar'2006, Dresden, Germany, August-September 2006.
 16. Haiping Wu, Long Chen, Joseph Manzano, Guang R. Gao, A User-Friendly Methodology for Automatic Exploration of Compiler Options, In the Proceedings of the 2006 International Conference on Programming Languages and Compilers (PLC'06), Las Vegas, USA, June 26-29, 2006.
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C. Books / Book Chapters / Notes Sets

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D. Patents

1. Title: Method for Interating Software Pipelining with Multithreading
Guang R. Gao, with Hongbo Rong, Alban Douillet, R. Govindarajan
Provisional Application No.: 60/507,043
Filing Date: Sept. 29, 2003
US patent application pending
2. Title: Method and Apparatus for Real-Time Multithreading
Guang R. Gao and Kevin Theobald
Provisional Application No.: 60/384,495
Filing Date: May 31, 2002
US patent application pending
3. Title: Method And Apparatus For Iterative Emulation Of Large Logic Circuits Containing Multiple Identical Logic Modules
Guang R. Gao, with Hirofumi Sakane, Levent Yakay, Vishal Karna, Clement Leung
Provisional Application No.: 60/512,376
Filed Date: November 17, 2003
US patent application pending

Section C: Services

For detailed information about this section, please refer to <http://www.capsl.udel.edu/>