CURRICULUM VITAE

NAME

GUANG R. GAO

OFFICE ADDRESS

Department of Electrical Engineering
140 Evans Hall
University of Delaware
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EDUCATION

Ph.D Degree in *Electrical Engineering and Computer Science*
Massachusetts Institutes of Technology, August 1986.
Member of Computational Structures Group at Laboratory of Computer Science, MIT, June 1982 to August 1986.

MS Degree in *Electrical Engineering and Computer Science*
Massachusetts Institutes of Technology, June 1982.

BS Degree in *Electrical Engineering*
Tsinghua University, Beijing.

PROFESSIONAL EXPERIENCE

University of Delaware
Newark, DE, USA.
Endowed Distinguished Professor, Department of Electrical and Computer Engineering, effective from Sept. 1st, 2005.

University of Delaware
Newark, DE, USA.
Professor, Department of Electrical and Computer Engineering, Sept. 1996 – Presentj.
Founder and leader of the Computer Architectures and Parallel Systems Laboratory (CAPSL).

McGill University
Montreal, Canada
Associate Professor, School of Computer Science, Jun. 1992 - Aug. 1996.
Assistant Professor, School of Computer Science, Aug. 1987 - Jun. 1992.
Founder and leader of the Advanced Compilers, Architectures and Parallel Systems Group (ACAPS) at McGill since 1988.

Center of Advanced Studies, IBM Toronto Lab
Aug. 1993 - Jun. 1994
Visiting scientist with a NSERC Senior Industrial Fellowship.

Philips Research Laboratories

Sept. 1986 - Jun. 1987.
Briarcliff Manor, NY, US.
Senior member of research staff of the Computer Architecture and Programming Systems Group. Played a major role in founding a multiprocessor system project, and research in parallelizing compilers.

Massachusetts Institutes of Technology

Jun. 1994 - Aug. 1994
Visiting Professor (Sabbatical)
Jun. 1980 - Aug. 1986
Member of the Computational Structures Group at the Laboratory of Computer Science, MIT.
Participated in the MIT Static Dataflow Architecture Project and other projects. Proposed a novel methodology of organizing array operations to exploit the fine-grain parallelism of dataflow computation models. Developed a unique pipelined code mapping scheme for dataflow machines (later known as dataflow software pipelining).

CURRENT RESEARCH AREAS

- Computer Architecture and Parallel Systems.
- Optimizing and Parallelizing Compilers.
- Runtime systems.
- Applications: Bio-Informatics and High Performance Computing.

PROFESSIONAL MEMBERSHIP

Senior Member of IEEE, Member of ACM, ACM-SIGARCH, ACM-SIGPLAN.

NATIONAL AND INTERNATIONAL RECOGNITION

- ACM Fellow.
- IEEE Fellow.
- IEEE Computer Society Distinguished Visitor, 1998-2001.
- Elected as a chairman of a collection of well recognized international conferences in computer/information sciences and engineering (see list).
- Invited as a Keynotes Speaker of a number of recognized international conferences (e.g. IPDPS 2005, HiPC2005, IWOMP2006, NPC2007, GCC2009).
- Elected as a Distinguished Professor of Electrical and Computer Engineering – with a Named Professorship at University of Delaware.

CITATIONS AND SPECIAL APPOINTMENTS

- Citation from IEEE Fellowship: For contributions to multiprocessor computers and compiler optimization techniques.
- Citations from ACM Fellowship: For contributions to architecture and compiler technology of parallel computers.
- Gao's publications have been cited widely in his field. For example, there are well over 500 citations for his top 5 most cited papers. Gao's work has attracted the attention of many researchers in diverse application areas. The impact of his work is apparent through the impact of his work in his areas and several modifications and extensions from of the approaches and algorithms pioneered by his work.

He has many special appointments – most are evident on the list of recognized international conferences where he has been appointed as chairman or technical program committee members, or editorships on prestigious journal as listed below.
He also has received honorable appointments. For example, he has served as a panelist of many international conference panels and National Science Foundation grant review panels, external Ph.D thesis examiners both within US and internationally (detailed list can be submitted on request). He also held honorable special visiting professorships in several universities in China – especially the prestigious Tsinghua University (since 2007).
Most recently, he has been invited to server in an international review panel in Computer Science field of Tsinghua University (together with 4 other internationally well recognized computer scientists – holding prestigious titles such National Academy of Enginnering (NAE) member, AAAS Fellow, Royal Academy of Engineering Fellow, Founder member of the Scientific Council of the European Research Council)

CONFERENCE COMMITTEE CHAIRMANSHIP

- Advisor Board, International Conference on Parallel Processing (Europar'12)
- Program Chairman of the 40th International Conference on Parallel Processing (ICPP'11), Taipei, Taiwan.
- Panel Coordinator, International Conference on Parallel Architectures and Compiler Technology (PACT 2011); Data-Flow Execution Models for Extreme Scale Computing (DFM 2011).
- Advisor Board, International Conference on Parallel Processing (Europar'11)
- Program Co-Chair of the 22nd Workshop on Language and Compilers for Parallel Computing (LCPC'10), Oct 2009 in Newark, DE,USA,
- Program Co-Chair of IFIP International Conference on Network and Parallel Computing (NPC'09), October 19 to 21, 2009 in Gold Coast, Australia
- Vice Program Chairman of the 36th International Conference on Parallel Processing (ICPP'07), September 10-14, 2007 in XiAn China
- Program Chairman of International Workshop on OpenMP (IWOMP'2007), June 3rd - June 7th, 2007 in Beijing, China
- General Chair of International Conference on Embedded and Ubiquitous Computing (EUC'04), August 26-28, 2004 in Aizu, Japan
- Program Co-Chair of IFIP International Conference on Network and Parallel Computing (NPC'04), Oct 18 - 20, 2004 in Wuhan, China
- Program Vice-Chair of International Parallel & Distributed Processing Symposium (IPDPS'04), April 30, 2004 in Santa Fe, New Mexico
- Program Vice-Chair of International Conference on High Performance Computing (HiPC'01), Dec 17 – 20, 2001 in The Taj Krishna in Hyderabad, India
- Program Co-Chair of the Compilers, Architectures and Synthesis for Embedded Systems (CASES'01), November 16 - 17, 2001 in Atlanta, Georgia, USA
- Chair of the Third Workshop on Petaflop Computing, Feb. 1999 in Annapolis, MD.
- Co-Chair of the Multithreaded Architecture Workshop, in Conjunction to HPCA'99, Jan. 1999 in Orlando, Florida
- General Co-Chair of the 1998 International Conference on Parallel Architectures and Compilation Techniques (PACT'98), Oct. 1998 in Paris, France., co-sponsored by IFIP and IEEE Computer Society
- Co-Chair of the Compiler and Architecture Support for Embedded Systems (CASES'98, 99), in Washington D.C.
- Program Chairman of the 1994 International Conference on parallel Architectures and Compilation Techniques (PACT'94), Aug. 1994 in Montreal, Canada.

JOURNAL EDITORSHIP

- Editorial Board of Journal of Chinese Computer Research and Development (2005 –)
- Editorial Board of the Journal of Embedded Computing (2004-)
- Editorial Board of the International Journal of High Performance Computing and Networking (2003 –)
- Parallel Processing Letters (2001-)
- Editorial Board of IEEE Transactions on Computers (1998 - 2001)
- Editorial Board of IEEE Concurrency Journal (1997 - 2000)
- Editorial Board of the Journal on Programming Languages in Jan. 1996, and subsequently became one of the two Co-Editors of the journal (1997-1998).
- Guest Editor for the Special Issue on IEEE Transaction on Computers, Journal of Parallel and Distributed Computing, etc.

PROGRAM COMMITTEE MEMBERS OF RECOGNIZED INTERNATIONAL CONFERENCES

- International Conference of Parallel Processing (ICPP'12).
- International Conference on Parallel Architectures and Compiler Technology (PACT 2012); Data-Flow Execution Models for Extreme Scale Computing (DFM 2011, 2012).
- IFIP International Conference on Network and Parallel Computing (NPC'04, 05, 06, 09, 10, 11, 12)
- International Workshop on Languages and Compilers for Parallel Computing (LCPC 2010, 2011, 2012).
- International Symposium on Code Generation and Optimization (CGO'11, CGO'12).
- International Workshop on OpenMP (IWOMP'06, 07, 08, 09, 10, 11, 12).
- Programming Language Design and Implementation (PLDI); Open64 Workshop'12.
- Programming Language Design and Implementation (PLDI); Multicore and GPU Programming Models, Languages and Compilers Workshop (PLC'12).
- ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP 2010).
- Workshop on Multithreaded Architectures and Applications (MTAAP 07, 08, 09, 10, 11, 12).
- IFIP and ACM SIGARCH International Conference on Parallel Architectures and Compilation Techniques (PACT'94, 95, 96, 97, 98, 99, 00, 01, 07, 10, 11, 12).
- IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES'06, 07, 08, 09, 10, 11).
- Workshop on Programmability Issues for Multi-Core Computers (MULTIPROG'08, 09, 10, 11, 12)
- International Conference on High-Performance Embedded Architecture and Compilation (HiPEAC 2009).
- ACM Computing Frontiers (CF 2008).
- Asia-Pacific Computer Systems Architecture Conference (ACSAC'06, 07, 08).
- International Conference on Parallel Processing (ICPP'07).
- ACM/IEEE International Conference for High Performance Computing and Communications (SC07, 08, 09, 10, 11).
- ACM/IEEE International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS 2007).
- ACM International Conference on Supercomputing (ICS'95, 02, 03, 04, 06, 07, 08).
- IEEE International Parallel and Distributed Processing Symposium (IPDPS'01, 02, 03, 06, 10).
- Fifth IEEE International Workshop on High Performance Computational Biology (HiCOMB'06).
- ACM International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN 2005).
- ACM/IEEE International Symposium on Micro architectures (MICRO'95, 96, 97, 02).
- High Performance Computing Symposium (HPCS'95, 96, 98, 99, 01, 02).
- International Conference on Parallel Processing (EURO-PAR'95, 96, 01).
- Compilers, Architectures and Synthesis for Embedded Systems (CASES'00, 01).
- IEEE International Symposium on High Performance Computer (HPCA'97, 99, 00).
- International Conference on Compiler Construction (CC'98, 99, 00), Europe.
- Working Conference on Massively Parallel Programming Models (MPPM'93, 95, 97, 99).

- International Symposium on High Performance Computing (ISHPC'99), Japan.
- ACM Symposium on Programming Language Design and Implementation (PLDI'98).
- International Parallel Processing Symposium (IPPS'95).
- IEEE International Conference on Algorithms and Architectures for Parallel Processing (ICAPP'95).
- Parallel Architecture and Language Europe (PARLE'91, 92, 93, 94, 95).

PANEL OF INTERNATIONAL CONFERENCES AND MEETINGS

Invited as a panel chair or a panelist in panels of many nternational conferences and meetings

INVITED SEMINARS AND DISTINGUISHED SEMINARS (Partial)

Given seminars in many industrial and academic organizations:

- IBMT.J. Watson Research Center
- IBM Toronto Lab,
- AT&T Bell Laboratories
- BNR
- HP Labs
- Intel
- SGI
- DEC
- QualComm
- NRL (Navy Research Lab.)
- JPL (Jet Propulsion Laboratory)
- Sandia National Laboratory
- Oak Ridge National Laboratory
- NASA Ames Research Center
- PNNL (Pacific Northwest National Laboratory)
- MIT
- Stanford University
- UC Berkeley
- NYU
- Cornell University
- University of Maryland
- University of Alberta
- University of Colorado
- University of Southern California
- University of Toronto
- University of Victoria
- University of Michigan

GRANTS AND OTHER REVIEW FUNCTIONS

- Invited as National Science Foundation (NSF) grant review panels (many times)
- Invited as an external reviewer of a grant reviewer to NSF-equivalent organizations in other countries (Canada, England, Holland, France, etc.)
- Invited as a reviewer for tenure and other promotion reviewers for professors/scientists both in US and beyond.
- Invited as external Ph.D thesis examiners both within US and internationally (e.g. INRIA (France), Chamers University (Sweden), Tsinghua University (China), Chinese University of Science and Technology (China), Huazhong University of Science and Technology (China), etc.).

Section A: Teaching and Research Supervision

A.1: TEACHING

A series of new courses have been introduced and taught over years. The topics include:

1. Computer Architectures
2. Parallel Computing
3. Parallel and Functional Programming
4. Optimizing and Parallelizing Compilers
5. Discovery Informatics and High-Performance Computing

For a detailed course listing, please see http://www.capsl.udel.edu/

A.2: RESEARCH SUPERVISION

Current, graduate students under my supervision include:

1. Mark Pellegrini (Performance Analysis).
2. Andrew Russo (TBD).
3. John Tully (TBD).
4. Wesley Toland (TBD).
5. Juergen Ributzka (Compilers) (2009 – 2013 Expected).
6. Brian Lucas (High Performance IO) (2007 – 2012 Master Expected).
7. Thomas St. John (Parallel Graph Algorithms) (2007 – 2012 Master Expected).
8. Chris Adamopoulos (Compilers) (2007 – Master Expected).
9. Kelly Livingston (Computer Architecture and Parallel Application) (2007 – 2013 Expected)
10. Sunil Shrestha (Compilers) (2007 – 2013 Expected).
11. Elkin Garcia (Parallel Applications) (2008 – 2012 Expected).
12. Joshua Suetterlein (TBD) (2010 – 2015 Expected).
13. Aaron M. Landwehr (TBD) (2010 – 2015 Expected).
14. Robert Pavel (Parallel Simulation) (2010 – 2015 Expected).
15. Joshua B. Landwehr (TBD) (2010 – 2012 Master Expected).

Current Postdoc fellows under my supervision include:

1. Stéphane Zuckerman (2010 – present).
2. Chen Chen (2011– present).
3. Souad Koliai (2012– present).

Already Completed:

The following Graduate students and Post-Docs have already completed their proposed research under my supervision:

PhD Level:

1. Daniel Orozco
   TIDeFlow: A Dataflow-nspired execution model for high performance computing programs
   University of Delaware (USA), 2007 – 2012.

2. Joseph B. Manzano
   A comparison between virtual code management techniques
   University of Delaware (USA), 2003 – 2011.

3. Ge Gan
Programming model and execution model for OpenMP on the Cyclops-64 manycore processor
University of Delaware (USA), 2004 – 2010.

4. Long Chen
Exploring novel many-core architectures for scientific computing
University of Delaware (USA), 2005 – 2010.

5. Fei Chen
Enabling system validation for the many-core supercomputer
University of Delaware (USA), 2001 – 2009.

6. Juan del Cuvillo
Breaking away from the OS shadow: A program execution model aware thread virtual machine for multicore architectures
University of Delaware (USA), 2001 – 2008.

7. Yuan Zhang
Static analyses and optimizations for parallel programs with synchronization
University of Delaware (USA), 2002 – 2008.

8. Mihailo Kaplarevic
Environmental genome informational utility system (EnGENIUS)
University of Delaware (USA), 2001 – 2007.

9. Weirong Zhu
Efficient synchronization for a large-scale multi-core chip architecture
University of Delaware (USA), 2002 – 2007.

10. Rishi Lee Khan
Engineering systems neuroscience: Modeling of a key adaptive brain control system involved in hypertension
University of Delaware (USA), 2000 – 2007.

11. Alban Douillet
A compiler framework for loop nest software-pipelining
University of Delaware (USA), 2001 – 2006.

12. Yanwei Niu
Parallelization and performance optimization of bioinformatics and biomedical applications targeted to advanced computer architectures
University of Delaware (USA), 2001 – 2005.

13. Robel Y. Kahsay
Advanced protein sequence analysis methods for structure and function prediction
University of Delaware (USA), 2001 – 2005.

14. Andres Marquez
The CARE architecture
University of Delaware (USA), 1995 – 2004.

15. Hongbo Yang
Power-aware compilation techniques for high performance processors
University of Delaware (USA), 1999 – 2003.

16. Parimala Thulasiraman
Irregular computations on fine-grain multithreaded architecture
University of Delaware (USA), 1995-2000.

17. Xinan Tang
Compiling for multithreaded architectures
University of Delaware (USA), 1995 – 1999.

18. Kevin Bryan Theobald
EARTH: An Efficient Architecture for Running Threads
McGill University (Canada), 1990 – 1999.

19. Erik Richter Altman
Optimal software pipelining with function unit and register constraints
McGill University (Canada), 1991 – 1996.

20. Shashank Nemawarkar
Performance modeling and analysis of multithreaded architectures
McGill University (Canada), 1989 – 1996.

21. Vugranam C. Sreedhar
Efficient program analysis using DJ graphs
McGill University (Canada), 1990 – 1995.

22. Guy Tremblay
Parallel implementation of lazy functional languages using abstract demand propagation
McGill University (Canada), 1988 – 1994.

23. Qi Ning
Register allocation for optimal loop scheduling
McGill University (Canada), 1990 – 1993.

24. Herbert H. J. Hum
The Super-Actor Machine: A hybrid dataflow/von Neumann architecture
McGill University (Canada), 1990 – 1992.

25. Robert Kim Yates
Semantics of timed dataflow networks
McGill University (Canada), 1988 – 1992.

MS Level:

1. Sunil Shrestha
Parallel Low-Overhead Data Collection Framework for a Resource Centric Performance Analysis Tool
University of Delaware (USA), 2007 – 2012.

2. Xiaomi An
Memory State Flow Analysis and Its Application
University of Delaware (USA), 2009 – 2011.

3. Juergen Ributzka
Toward a software pipelining framework for many-core chips
University of Delaware (USA), 2005 – 2009.

4. Jonathan L. Barton
Hardware implementation of a synchronization state buffer in VHDL
University of Delaware (USA), 2005 – 2008.

5. Mark Pellegrini
A case study of the Mstack cross-platform benchmark on the Cray MTA-2
University of Delaware (USA), 2004 – 2008.

6. Matthew Wells
University of Delaware (USA), 2006 - 2008.

7. Yi Jiang
Design and implementation of tool-chain framework to support OpenMP single source compilation on cell platform
University of Delaware (USA), 2006 – 2008.

8. Long Chen
Optimizing the Fast Fourier Transform on a many-core architecture
University of Delaware (USA), 2005 – 2008.

9. Liping Xue
Efficient mapping of fast Fourier transform on the Cyclops-64 multithreaded architecture
University of Delaware (USA), 2005 – 2007.

10. Ge Gan
CDP: A multithreaded implementation of a network communication protocol on the Cyclops-64 multithreaded architecture
University of Delaware (USA), 2004 – 2007.

11. Eun Jung Park
Methodology of dynamic compiler option selection based on static program analysis: Implementation and evaluation
University of Delaware (USA), 2004 – 2007.

12. Dimitrij Krepis
A study of simulation and verification of a many-core architecture on two modern reconfigurable platforms
University of Delaware (USA), 2004 – 2007.

13. Divya Parthasarathi
Tower methodology for verification of multi-core architecture: A case study
University of Delaware (USA), 2003 – 2005.

14. Ying Ping Zhang
A study of architecture and performance of IBM Cyclops64 interconnection network
University of Delaware (USA), 2003 – 2005.

15. Vishal Karna
Multiprocessor SOC Verification
University of Delaware (USA), 2002 – 2005.

16. Robert Klosiewics
A Parallel Debugger for the Cyclops Architecture
University of Delaware (USA), 2002 – 2004.

17. Inanc Dogru
An integer linear programming approach to reduce register spills on itanium processors
University of Delaware (USA), 2002 – 2004.

18. Xing Wang
Quantitive Study of Human-Computer interaction in adaptive search on Mobile Handsets and its Localization for Mandarin Chinesse
University of Delaware (USA), 2001 – 2004.

19. Weirong Zhu
Multithreaded Parallel Implementation of HPMMPFAM on EARTH
University of Delaware (USA), 2001 – 2004.

20. Fei Chen
Implementing Parallel CG Algorithm on the EARTH Multithreaded Architecture
University of Delaware (USA), 2001 – 2004.

21. Yan Xie
Code Size Oriented Memory Allocation for Temporary Variables
University of Delaware (USA), 2001 – 2003.

22. Chuan Shen
A Portable Runtime System and its Derivation for the Hardware SU Implementation
University of Delaware (USA), 2001 – 2003.

23. Kapil Khosla
Binary Diffing
University of Delaware (USA), 2001 – 2003.

24. Tamal Basu
Survivability of routing protocols in large scale clustered fractal networks
University of Delaware (USA), 2001.

25. Rishi Kumar
Efficient Parallelization of Reductions and Loop Based Programs on EARTH
University of Delaware (USA), 1999 – 2001.

26. Praveen Thiagarajan
A Visual Perspective to Motif/Pattern Analysis
University of Delaware (USA), 1999 – 2001.

27. Juan. Del. Cuvillo
Whole Genome Comparison Using A Multithreaded Parallel Implementation
University of Delaware (USA), 1999 – 2001.

28. Christopher J. Morrone
A EARTH Runtime System For Multi-Processor/Multi-Node Beowulf Cluster
University of Delaware (USA), 1999 – 2001.

29. Alban Douillet
Register Stack and Optimal Allocation Instruction Placement
University of Delaware (USA), 1999 – 2001.

30. Sean Ryan
Developing a software distributed shared memory for the EARTH platform
University of Delaware (USA), 1999 – 2000.

31. Kamala Prasad Kakulavarapu
Dynamic load balancing issues in the EARTH runtime system
McGill University (Canada), 1996 – 2000.

32. Ian Stuart MacKenzie Walker
Towards a Custom EARTH Synchronization Unit
University of Delaware (USA), 1998 – 1999.

33. Cheng Li
Earth-SMP: multithreading support on an SMP cluster
University of Delaware (USA), 1997 – 1999.

34. Lei Liu
The effect of resource complexity on modulo scheduling
University of Delaware (USA), 1997 – 1999.

35. Maria-Dana Tarlescu
The elastic history buffer: A multi-hybrid branch prediction scheme using static classification
McGill University (Canada), 1996 – 1999.

36. Dionis Hristov
Development of tests for the ATM signaling protocol
McGill University (Canada), 1998.

37. Hisham Johnathon Petry
Comparison of SC derived memory models and location consistency on shared memory architectures
McGill University (Canada), 1995 – 1997.

38. Haiying Cai
Dynamic load balancing on the EARTH-SP system
McGill University (Canada), 1997.

39. Raul Esteban Silvera-Munoz
Static instruction scheduling for dynamic issue processors
McGill University (Canada), 1996 – 1997.

40. Shaohua Han
Implementation of nested relations in a database programming language
McGill University (Canada), 1996 – 1997.

41. Hongru Cai
McGill University (Canada), 1995 – 1997.

42. Artour V Stoutchinin
Optimal software pipelining: Integer linear programming approach
McGill University (Canada), 1994 – 1996.

43. Shamir Fatehali Merali
Designing and implementing memory consistency models for shared-memory multiprocessors
McGill University (Canada), 1993 – 1996.

44. Alberto Jimenez
McGill University (Canada), 1993 – 1996.

45. Nasser Elmasri
TCL: Experiences ona multiprocessor with dual-processor nodes
McGill University (Canada), 1992 – 1995.

46. Renhua Wen
The design and implementation of an accurate array data-flow analyzer in the HPC compiler
McGill University (Canada), 1993 – 1995.

47. Luis Alfonso Lozano
Exploiting short-lived variables in superscalar processors
McGill University (Canada), 1992 – 1994.

48. Chandrika Mukerji
Register allocation using cyclic interval graphs
McGill University (Canada), 1991 – 1994.

49. M Ravi Shanker
A parallel implementation of the A-Viterbi algorithm for speech recognition*
McGill University (Canada), 1991 – 1993.

50. Cecile Moura (1991 - 1993)
SuperDLX - A Generic Superscalar Simulator
McGill University (Canada), 1991 – 1993.

51. Qi Ning
Register allocation for optimal loop scheduling
McGill University (Canada), 1991 – 1993.

52. Russell Olsen
Collective Loop Fusion for Array Contraction
McGill University (Canada), 1989 – 1992.

53. Nematollaah Shiri-Varnaamkhaasti
A design and implementation of unimodular transformations of loops
McGill University (Canada), 1990 – 1992.

54. Yue-Bong Wong
A petri-net model for loop scheduling
McGill University (Canada), 1989 – 1991.

55. Jean-Marc Monti
Interprocessor communication supports for a multiprocessor dataflow machine
McGill University (Canada), 1989 – 1991.

56. Alan Emtage
McGill University (Canada), 1988 – 1991.

57. Zaharias Paraskevas
Code generation for dataflow software pipelining
McGill University (Canada), 1987 – 1989.

Postdoc:

1. Xiaoxuan Meng (2009 – 2011).
2. Handong Ye (2008 – 2009).
3. Yeonseok Lee (2007 – 2008).
4. Jean Christophe Beyler (2007 – 2008).
5. Ziang Hu (1999 – 2008).
6. Haiping Wu (2000 – 2008).
7. Ioannis E. Venetis (2006 – 2007).
8. Shuxin Yang (2005 – 2007).
9. Ted T. Jeong (2005 – 2006).
10. Hongbo Rong (2001 – 2005).
11. Hirofumi sakane (2001 – 2005).
12. Andres Marquez (2004).
13. Jozsef bukszar (2002 – 2004).
14. Jizhu Lu (2000 – 2004).
15. Jianshan Tang (2002 – 2003).
16. Rongcai Zhao (2000 – 2001).
17. José N. Amaral (1998 – 2000).
18. Ruppa Thulasiraman (1998 – 2000).
19. Gerd Heber (1997 – 1999).
20. Chihong Zhang (1998 – 1999).
21. Olivier Maquelin (1994 – 1998).
22. Jian Wang (1995 – 1997).
23. Xinmin Tian (1993 – 1996).
24. Benoit Dupont Dinechi (1995 – 1996).
25. Ramaswamy Govindarajan (1990 – 1994).
26. Guoning Liao (1991 – 1993).

Those who have graduated are trained in the field of parallel architectures and compilers, as evidenced by the fact that they have been working (or worked) as tenure-track university professors (Ramaswamy Govindarajan, Guy Tremblay, José N Amaral, Parimala Thulasiraman, Ruppa Thulasiraman) as engineers in key industrial sectors, e.g., Intel (Herbert H. J. Hum, Xinmin Tian, Prasad Kakulavarapu, Shaohua Han, Kevin B. Theobald, Ian Walker, Sean Ryan, Divya Parthasarathi, Yingping Zhang), Nortel (Jian Wang), IBM (Erik R. Altman, Shashank Nemawarkar, Vugranam C. Sreedhar, Rauls Silvera), Microsoft (Hongbo Rong, Weirong Zhu, Yuan Zhang), BNR (Guoning Liao, Renhua Wen), HP (Luis A. Lozano, Alban Douillet, Shuxin Yang), Convex (Qi Ning), NCUBE (Russell Olsen), CAE (Nasser Elmasri), AT&T (Hisham J. Petry), Quallcom (Vishal Karnal, Rishi Kumar, Chihong Zhang) and as researchers in government labs, e.g., LLNL (Robert K. Yates, Christopher J. Morrone), PNNL (Andrés Marquez), or assuming other professional jobs.

Section B: Scholarship

B.1: RESEARCH ACTIVITY AND INTERESTS

1. Computer Architecture and Parallel Systems

There are a number of topics Gao has made important contributions that have great impact in the field. To name a few: (1) multithreaded architecture models and features leading/ pioneered the conception and design of a unique fine-grain multithreaded architecture based on static dataflow models - the well-known EARTH (Efficient Architecture for Running THreads) model; EARTH has applied the principles of dataflow computation principles to parallel computer architectures built from commodity components while demonstrating a migration path from commodity to custom hardware technology for scalable performance – the lasting impact of which will be appreciated even more when the emerging technology revolution of multi-core chips will need to deal with similar issues on fine-grain parallelism that EARTH has addressed in the past; (2) a novel memory consistency model (i.e. the Location Consistency) -- a new memory model for shared

memory machines that allows the implementation of an efficient cache coherence protocol which avoids invalidation traffic and requires neither bus snooping, nor directories; (3) novel architecture features exploring instruction-level parallelism (e.g. superscalar architecture support of short-lived variables, the fundamental notion of instruction-level parallelism smoothability and others.

2. Optimizing and Parallelizing Compilers

There are a number of topics Gao has made important contributions that have great impact in this field. To name a few: program analysis techniques (e.g. fast algorithms to compute and apply SSA form, loop nests optimization (e.g. collective loop fusion and optimization) and instruction scheduling and register allocation (e.g. register allocation based on interval graphs), and software pipelining. Software pipelining is one of the most important compiler technologies for the exploitation of instruction-level parallelism in code optimization for modern microprocessor architectures. Gao's contribution to software pipelining area is very impressive. Gao's work is unique as he has proposed to viewed the software pipelining problem from the angle of a dataflow program graph model that has led interesting and distinct paths to formulate and solve some of the hard problems facing software pipelining. For example, his work on inner-most loop software pipelining pioneered a novel integer linear programming based methodology to solve the scheduling and register allocation problems in software pipelining, and his most recent work by extending software pipelining for nested loops [see his ACM PLDI2005 paper (ftp://ftp.capsl.udel.edu/pub/doc/papers/SSP-RegAlloc.pdf) and IEEE/ACM CGO 2004 papers (ftp://ftp.capsl.udel.edu/pub/doc/papers/SSP-Scheduling.pdf, ftp://ftp.capsl.udel.edu/pub/doc/papers/SSP-CodeGen.pdf) have opened a new path to exploit parallelism for nested loops.

3. Runtime systems

In recent years, the elements required to design a successful computer system have been unified with the introduction of the execution model theory. G.R. Gao has devoted a significant part of his career to lead cutting edge research on the field of execution models. Gao has shown that Runtime Systems are essential to support execution models by enforcing and supporting the semantics of programs. Gao's work has resulted in prominent contributions to the field, including the development of runtime systems to support the execution of programs as required by DARPA's Ubiquitous High Performance Computing (UHPC) project. In the UHPC project, Gao has been in charge of designing the system software, the runtime system and the execution models. Gao's work on runtime systems has resulted in numerous scientific papers and several awards. For example, his work on execution models has lead new models such as The Time Iterated Dependency Flow Execution Model (TIDeFlow), designed for efficient development of high performance parallel programs for many-core architectures [http://www.capsl.udel.edu/pub/doc/papers/DFM2011-Orozco.pdf]. Gao has also received the 2011 Gauss Award, an international award recognizing the most outstanding research paper in the field of scalable supercomputing [http://www.udel.edu/udaily/2012/aug/gao-gauss-award-080411.html]. Gao's work on dynamic scheduling and energy aware optimizations has been extensively published and awarded at international conferences [See IPDPS-MTAAP http://www.capsl.udel.edu/pub/doc/papers/garcia-mtaap2012.pdf and the best paper award at Hipeac-MULTIPROG http://www.capsl.udel.edu/pub/doc/papers/MULTIPROG2010-Garcia.pdf]

4. Applications: Bio-Informatics and High Performance Computing

Our long-term research goal is to apply high-performance computing technology to remove road blocks in solving critical problems in bioinformatics. We recognize that a main challenge is providing biologists with a smooth interactive solution platform for knowledge discovery from large data sets which, unfortunately, are grossly incomplete and have a considerable amount of errors. CAPB consists of researchers with strong computer engineering and computer science backgrounds who are eager to collaborate with researchers from other fields, and are dedicated to finding innovative solutions to meet the above challenges.

B.2: LIST OF RESEARCH PUBLICATIONS

The contributions are listed under the following category:

Referred Journal Publications
Referred Conference Publications
Books/ Book Chapters/ Notes Sets
Patents

A. Referred Journal Publications

1. Daniel Orozco, Elkin Garcia, Rishi Khan, Kelly Livingston and Guang R. Gao. Toward High Throughput Algorithms on Many Core Architectures. ACM Transactions on Architecture and Code Optimization (TACO), Volume 8, Issue 4, January 2012, Article No. 49.
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209. G. R. Gao and S. J. Thomas, An optimal parallel Jacobi-like solution method for the singular value decomposition, Proceedings of the International Conference on Parallel Processing, Pages: 47–53, University Park, PA, USA, August 10-14 1988.
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211. Jack B. Dennis, Guang R. Gao, Maximum Pipelining of Array Operations on Static Data Flow Machine, Proceedings of International Conference on Parallel Processing (ICPP'83), Pages: 331-334, Columbus, Ohio, USA, 1983.

C. Books / Book Chapters / Notes Sets

1. L.T.Yang, M. Guo, G. R. Gao, N. K. Jha, Proceedings of Embedded and Ubiquitous Computing, International Conference EUC 2004, Aizu-Wakamatsu City, Japan, August 25-27, 2004, Lecture Notes in Computer Science, Vol. 3207. Springer, 2004.
2. B. Kleinjohann, G. R. Gao, H. Kopetz, L. Kleinjohann and A. Rettberg, Design Methods and Applications for Distributed Embedded Systems, IFIP International Federation for Information Processing , Vol. 150. Springer 2004.
3. Hai Jin, Guang R. Gao, Zhiwei Xu, Hao Chen (Eds.), Proceedings of Network and Parallel Computing, IFIP International Conference, NPC 2004, Wuhan, China, October 18-20, 2004,. Lecture Notes in Computer Science 3222. Springer, 2004.
4. Guang R. Gao, Ken Arnold and Sudipto Ghosh, Java/Jini Technologies and High-Performance Pervasive Computing, 30 July and 1 August 2002, Boston, USA.
5. Krishna Palem, Guang R. Gao, Trevor Mudge, Proceedings of the 2001 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, Atlanta, Georgia, USA, November 16 - 17, 2001.
6. Guang R. Gao, J-L. Gaudiot, and L. Bic, editors, Advanced Topics in Dataflow and Multithreaded Computers. IEEE Computer Society Press, 1995.

7. Michel Cosnard, Guang R. Gao, Gabriel M. Silberman, Parallel Architectures and Compilation Techniques: Proceedings of the IFIP WG10.3 Working Conference, PACT '94, Montreal, Canada, 24-26 August 1994.
8. Jack B. Dennis and Guang R. Gao, Multithreaded Architectures: Principles, Projects, and Issues, In Robert A. Iannucci, Guang R. Gao, Robert H. Halstead, Jr., and Burton Smith, editors, Multithreaded Computer Architecture: A Summary of the State of the Art, chapter 1, Pages: 1-72. Kluwer Academic Publishers, Norwell, Massachusetts, 1994.
9. Robert A. Iannucci, Guang R. Gao, Robert H. Halstead, Jr., and Burton Smith, editors, Multi-threaded Computer Architecture: A Summary of the State of the Art. Kluwer Academic Publishers, Norwell, Massachusetts, 1994. Book contains papers presented at the Workshop on Multithreaded Computers, Albuquerque, New Mexico, November 1991.
10. Lenore M. R. Mullin, Michael J. Jenkins, Gaétan Hains, Robert Bernecky and Guang Gao, Arrays, Functional Languages, and Parallel Systems, Kluwer Academic Publishers, Boston, Massachusetts, December 1991.
11. Guang R. Gao, A Code Mapping Scheme for Dataflow Software Pipelining, Kluwer Academic Publishers, Boston, Massachusetts, December 1990.

D. Patents

1. Title: Runspace method, system and apparatus
   Rishi Khan, Daniel Orozco, Guang R. Gao.
   Patent No. US 2011/0246823 A1
   Date of Patent: Oct. 6, 2011

2. Title: Task-Oriented Node-Centric Checkpointing (TONCC)
   Rishi Khan, Guang R. Gao, Apperson H. Jhonson
   Patent No. US 2011/0246823 A1
   Date of Patent: Oct. 6, 2011

3. Title: Systems and Methods for Logic Verification
   Guang R. Gao, Fei Chen
   Patent No. US 7.934.179 B2
   Date of Patent: April 26, 2011

4. Title: Methods and Products for Processing Loop Nests
   Hongbo Rong, Guang R. Gao, Alban Douillet, R. Govindarajan
   Patent No. US 7.631.305 B2
   Date of Patent: Dec. 8, 2009

5. Title: Data driven logic simulation chip and tool chain
   Fei Chen, Guang R. Gao
   Patent No. US 2009/0222252 A1
   Date of Patent: Sep 3, 2009

6. Title: Methods and Apparatus for emulation of logic circuits
   Hirofumi Sakane, Levent Yakay, Vishal Karma, Clement Leung, Guang R. Gao.
   Patent No. US 7.356.454 B2
   Date of Patent: April 8, 2008

7. Title: Method for Integrating Software Pipelining with Multithreading
   Guang R. Gao, with Hongbo Rong, Alban Douillet, R. Govindarajan
   Provisional Application No.: 60/507,043
   Filing Date: Sept. 29, 2003
   US patent application pending

8. Title: Method and Apparatus for Real-Time Multithreading

Guang R. Gao and Kevin Theobald
Patent No. US 2005/0188177 A1
Date of Patent: Aug. 25, 2005

9. Title: Method And Apparatus For Iterative Emulation Of Large Logic Circuits Containing Multiple Identical Logic Modules
Guang R. Gao, with Hirofumi Sakane, Levent Yakay, Vishal Karna, Clement Leung
Provisional Application No.: 60/512,376
Filed Date: November 17, 2003
US patent application pending

B.3: CONTRACTS AND GRANTS

A. NSF Grants

1. SHF: MEDIUM: Collaborative Research: Architecture, Programmability, and Performance of Large Scale Parallel Systems. 2011-2014. NSF CCF-1065448. In charge $301,133
2. Collaborative Research: Programming Models and Storage System for High Performance Computation with Many-Core Processors. 2009-2012. NSF CCF-937907. In charge $299,984
3. A High Throughput Massive I/O Storage Hierarchy for PETA-scale High-end Architectures. 2009. NSF CCF-930078. In charge 12,000
4. Advanced Software Technology for an Exascale Point Design Study. 2009-2011. NSF CCF-925863. In charge $199,998.
5. Collaborative Research: PetaApps: Enabling Multiscale Modeling of Turbulent Clouds on Petascale Computers. 2009-2011. NSF OCI-904534. In charge 1,064,500
6. Collaborative Research: Programming Models, Compiles, and Runtimes for High-end Computing on Manycore Processors. 2008-2011. NSF CCF-833122. In charge $400,000
7. CSR-AES: Optimizations for Optimistic Parallelization Systems. 2007-2008. NSF CNS-720531. In charge $300,000
8. CRI: Planning a Research Compiler Infrastructure Based on Open64. 2007-2008. NSF CNS-708856. In charge $50,000
9. Collaborative Research: CRI: IAD: Development of a Research Infrastructure for the Multithreaded Computing Community Using the Cray Eldorado Platform. 2007-2013. NSF CNS-708820. In charge 77,150.
10. A High Throughput Massive I/O Storage Hierarchy for PETA-scale High-end Architectures. 2007-2010. NSF CCF-702244. In charge $311,999
11. Collaborative Research: A programmable, efficient and dynamic architecture and compilation Framework for Networking Applications. 2005-2006. NSF CCF-541002. In charge $175,000.
12. CSR-AES: Dynamic Adaptive Multithreading: Continous Compilation and Runtime Scheduling for High End Computing. 2005-2007. NSF CNS-509332. In charge $749,999.
13. A novel approach of software pipelining of multidimensional loops. 2004-2007. NSF 429781. In charge $122.350. Total $300.000
14. A meta-genome level analysis of an extreme microbial symbiosis. 2002-2005. NSF 120648. In charge $224.400. Total 1.501.886
15. Increasing parallel program performance with the LC Memory consistency model. 2001-2004. NSF CCR-0105540. In charge $86.898. Total $270.000
16. A framework for developing complex applications on high-end peta-flop-class machines. 2001-2004. NSF NGS-0103723. In charge $521.174. Total $1.100.000
17. Multithreading: A viable approach for single-chip architecture. 199-2002. NSF MIPS-0073527. In charge $187.998. Total $600.000
18. Configurable off-the-shelf multithreaded experimental testbed (COMET). 2000-2002. NSF 9986043. In charge $79.791. Total $79.791
19. CISE Postdoctoral Research Associate. 1999-2001 NSF 9901553. In charge $60.672. Total $60.672
20. Parallel and distributed computing: System and application development. 1997-2002. NSF CDA-9703088. In charge $633.513. Total $633.513

21. Crack Propagation on Teraflop Computers. NSF CISE-9726388. 1998-2000. In charge $264.952. Total $1.800.000
22. Compiling Irregular multithreaded architecture. NSF 9808522. 1998-2001. In charge $100.000. Total 319.156
23. New Generation Multithreaded processor. NSF MIPS-9707125. 1997-2000. In charge $187.417. Total $400.000
24. A Framework of modulo Scheduling Based on Finite Automaton. NSF CCR-9711477. 1997-1999. In Charge $139.263. Total $139.263.

B. Other Federal Grants.

1. Runnemede: Ubiquitous High Performance Computing (UHPC). 2010-2014. DARPA/Intel. In charge $995,984
2. A Robust Hybrid I/O Storage Hierarchy for Future High-End Computer Systems. 2007-2009. NSA. In charge $571,906
3. Dynamic Adaptive Execution Model for High Productivity Computing. 2008-2010. LSU/NSA. In charge $352,397
4. A dynamic Multithreaded Virtual Machine for High-End Computing: Architecture Model and Continuous Compilation. 2005-2006. NSA. In charge $468,367.
5. Design and Implementation of Virtual Feel Guided Mechanism; High Performance Micro Sensor Circuit Design. 2005-2006. NASA. In charge $25,000
6. A dynamic multithreaded virtual machine for high-end computing. 2005-2007. NSA. In charge $944.302. Total $944.302
7. Efficient architecture and compiler support for fine-grain multithreading. 2003-2005. NSA. In charge $945.000. Total $945.000
8. A programming model and software infrastructure. 2001-2003. NSA. In charge $444.000. Total $444.000
9. Computational genomics of complex adaptive integration. 2002-2005. NHI/NIGMS P20 GM67266-03. Total $1.920.000
10. Center for programming models for scalable parallel computing. 2002-2005. DOE DE-FC02-01ER25503. In charge $600.000. Total $9.000.000.
11. Multi-Tera Scale Complex Adaptation. 2001-2005 DARPA #F30602-01-2-0578.Total $1.548.000
12. Compiler Optimization. 2000-2002. DARPA/PAC/C. In charge $134.344. Total $9.000.000
13. Productive easy-to-use, reliable computing system. 2003-2006. DARPA/IBM. In charge $ 540.000. Total $53.000.000
14. Data Intensive Architcture (DIVA). 1999-2001. DARPA/AFSOR. In Charge $366.500 Total $12.000.000.
15. Hybrid Technology Multithreaded Architecture for Petaflops. 1997-2001. DARPA/NSA/NASA/NSF. In charge $1.363.000 Total $10.000.000

C. Industry Grants/Gifts and state funding

1. Cyclops Supercomputer System Software R&D Project. 2008-2009. ETI. In charge $54,315
2. Emerging Multi-Core Chip Hardware and Software Project. 2006-2007. ETI. In charge $60,000.
3. A Multi-Core Virtual Machine and IP Core. 2006. ETI. In charge $27,000
4. Cyclops Supercomputer System Software R&D Project. 2004-2005. ETI. In charge 160,019
5. Industry contracts and gifts (Intel, SGI, Connexant, AstroZenica, ETI, Acorn, Dupont, etc). 1996-2005. In charge $500.000
6. State funding. 1996-2005. DBI. In charge $93.000 Total $93.000

Section C: Services

C.1: UNIVERSITY ACTIVITIES AND SERVICES

- Member, Undergraduate award Committee (2006 –).
- Member, Faculty Strategic Planning Committee, ECE Dept. (2009 –).
- Member, Faculty Recruit Committee (1998 – 2008).
- Chair, Secondary Appointment Committee, ECE Dept. (2006 – 2007).
- Mmeber, Department recruiting committee (2004-2005).
- Member, Secondary Appointment Committee (2004-2005).
- Participating faculty retreat meeting (1998).
- Dean's ad hoc group for supercomputing (1998).
- Participate Engineering Outreach program.
- An advisor in the university Undergraduate Research Opportunity program.
- Chairing the departmental Committee on Promotion & Tenure (1998).
- College Election Committee (1998).
- Dean search committee.
- Graduate study and PhD exam revision committee (2001-2005).
- Ad Committee of Educational in Bioinformatics.
- DBI Scientific Committee.
- ICRSS committee (Instructional, Computing and Research Support Services Committee).

Section D: News

- News of Prof. Gao and CAPSL are available on the web. Visit http://www.capsl.udel.edu/news.shtml