

GUANG R. GAO

University of Delaware

Department of Electrical and Computer Engineering

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ggao.capsl@gmail.com<http://www.capsl.udel.edu/~ggao/>**EDUCATION**

- PhD** Degree in *Electrical Engineering and Computer Science* Massachusetts Institutes of Technology, August 1986.
Member of Computational Structures Group at Laboratory of Computer Science, MIT, June 1982 to August 1986.
- MS** Degree in *Electrical Engineering and Computer Science* Massachusetts Institutes of Technology, June 1982.
- BS** Degree in *Electrical Engineering* Tsinghua University, Beijing.

PROFESSIONAL EXPERIENCE

University of Delaware

Newark, DE, USA.

Endowed Distinguished Professor, Department of Electrical and Computer Engineering, effective from Sept. 1st, 2005.**University of Delaware**

Newark, DE, USA.

Professor, Department of Electrical and Computer Engineering, Sept. 1996 – Present.
Founder and leader of the Computer Architectures and Parallel Systems Laboratory (CAPSL).**McGill University**

Montreal, Canada

Associate Professor, School of Computer Science, Jun. 1992 --- Aug. 1996.

Assistant Professor, School of Computer Science, Aug. 1987 --- Jun. 1992.

Founder and leader of the Advanced Compilers, Architectures and Parallel Systems Group (ACAPS) at McGill since 1988.

Center of Advanced Studies, IBM Toronto Lab

Aug. 1993 --- Jun. 1994.

Visiting scientist with a NSERC Senior Industrial Fellowship.

Philips Research Laboratories

Sept. 1986 --- Jun. 1987.

Briarcliff Manor, NY, US.

Senior member of research staff of the Computer Architecture and Programming Systems Group. Played a major role in founding a multiprocessor system project, and research in parallelizing compilers.

**Massachusetts Institutes of
Technology**

Jun. 1994 --- Aug. 1994

Visiting Professor

(Sabbatical) Jun. 1980 --- Aug.

1986

Member of the Computational Structures Group at the Laboratory of Computer Science, MIT.

Participated in the MIT Static Dataflow Architecture Project and other projects. Proposed a novel methodology of organizing array operations to exploit the fine---grain parallelism of dataflow computation models. Developed a unique pipelined code mapping scheme for dataflow machines (later known as dataflow software pipelining).

CURRENT RESEARCH AREAS

- High Performance Computing and Dataflow Models
- Parallel Architecture and Systems
- Runtime systems and compilers
- Program mapping and optimization under dataflow models

PROFESSIONAL MEMBERSHIPS

- Member of IEEE/CS
- Member of ACM/SIGARCH
- Member of ACM/SIGPLAN.

NATIONAL AND INTERNATIONAL RECOGNITION

- ACM Fellow
- IEEE Fellow
- Endowed Named Professor of Electrical and Computer Engineering at University of Delaware
- CCF (Chinese Computer Federation) Outstanding Achievement Award of Overseas Scholars (One awardee per year)
- Chairmanship of a collection of well recognized international conferences in computer/information sciences and engineering (see list).
- Invited as a Keynotes Speaker of a number of recognized international conferences

CITATIONS AND SPECIAL APPOINTMENTS

- Citation from IEEE Fellowship: **For contributions to multiprocessor computers and compiler optimization techniques.**
- Citations from ACM Fellowship: **For contributions to architecture and compiler technology of parallel computers.**
- Gao's publications have been cited widely in his field visible via Google Scholar citation indices. Gao's work has attracted world in his research domain.
- Gao held honorable special visiting professorships in several universities in China – especially the prestigious Tsinghua University.

CONFERENCE COMITEE CHAIRMANSHIP (Served, a partial list)

- International Conference on Parallel Processing (ICPP)
- Panel Coordinator, International Conference on Parallel Architectures and Compiler Technology (PACT)
- DataFlow Execution Models for Extreme Scale Computing (DFM).
- International European Conference on Parallel and Distributed Computing (Europar)
- Workshop on Language and Compilers for Parallel Computing (LCPC')
- IFIP International Conference on Network and Parallel Computing (NPC)
- International Workshop on OpenMP
- International Conference on Embedded and Ubiquitous
- International Parallel & Distributed Processing Symposium (IPDPS)
- International Conference on High Performance Computing (HiPC)
- Compilers, Architectures and Synthesis for Embedded Systems (CASES)
- Workshop on Petaflop Computing
- Multithreaded Architecture Workshop, in Conjunction to HPCA

JOURNAL EDITORSHIP (served, a partial list)

- Editorial Board of Journal of Chinese Computer Research and Development
- Editorial Board of the Journal of Embedded Computing
- Editorial Board of the International Journal of High Performance Computing and Networking
- Parallel Processing Letters
- Editorial Board of IEEE Transactions on Computers
- Editorial Board of IEEE Concurrency Journal
- Editorial Board of the Journal on Programming Language
- IEEE Transaction on Computers
- Journal of Parallel and Distributed Computing

**PROGRAM COMMITTEE MEMBERS OF RECOGNIZED INTERNATIONAL
CONFERENCES (served, partial list)**

- International Conference of Parallel Processing (ICPP).
- International Conference on Parallel Architectures and Compiler Technology (PACT)
- DataFlow Execution Models for Extreme Scale Computing (DFM).
- IFIP International Conference on Network and Parallel Computing (NPC)
- International Workshop on Languages and Compilers for Parallel Computing (LCPC).
- International Symposium on Code Generation and Optimization (CGO).
- International Workshop on OpenMP (IWOMP)
- Programming Language Design and Implementation (PLDI)
- Multicore and GPU Programming Models, Languages and Compilers Workshop (PLC).
- ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP)
- Workshop on Multithreaded Architectures and Applications (MTAAP)
- IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES)
- Workshop on Programmability Issues for MultiCore Computers (MULTIPROG)
- International Conference on High-Performance Embedded Architecture and Compilation (HiPEAC).
- ACM Computing Frontiers (CF)
- Asia-Pacific Computer Systems Architecture Conference (ACSAC).
- ACM/IEEE International Conference for High Performance Computing and Communications (SC).
- ACM/IEEE International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS).
- ACM International Conference on Supercomputing (ICS).
- IEEE International Parallel and Distributed Processing Symposium (IPDPS).
- Fifth IEEE International Workshop on High Performance Computational Biology (HiCOMB).
- ACM International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN)
- ACM/IEEE International Symposium on Micro architectures (MICRO).
- High Performance Computing Symposium (HPCS).
- International Conference on Parallel Processing (EUROPAR).
- Compilers, Architectures and Synthesis for Embedded Systems (CASES).
- IEEE International Symposium on High Performance Computer (HPCA).
- International Conference on Compiler Construction (CC)
- Working Conference on Massively Parallel Programming Models (MPPM)
- International Symposium on High Performance Computing (ISHPC)
- International Parallel Processing Symposium (IPPS)
- IEEE International Conference on Algorithms and Architectures for Parallel Processing (ICAPP)
- Parallel Architecture and Language Europe (PARLE).

PANEL OF INTERNATIONAL CONFERENCES AND MEETINGS

Invited as a panel chair or a panelist of many international conferences and meetings.

INVITED SEMINARS AND DISTINGUISHED SEMINARS (Partial)

Given seminars in many industrial and academic organizations in USA and Canada

- IBMT.J. Watson Research Center
- IBM Amadan Research Center
- IBM Santa Teresa Lab.
- IBM Toronto Lab,
- AT&T Bell Laboratories
- BNR
- HP Labs
- Intel
- SGI
- DEC
- QualComm
- NRL (Navy Research Lab.)
- JPL (Jet Propulsion Laboratory)
- ANL (Argonne National Lab)
- Sandia National Laboratory
- Oak Ridge National Laboratory
- NASA Ames Research Center
- PNNL (Pacific Northwest National Laboratory)
- MIT
- Stanford University
- UC Berkeley
- NYU
- Cornell University
- University of Maryland
- University of Alberta
- University of Colorado
- University of Illinois
- University of Southern California
- University of Toronto

- University of Victoria
- University of Michigan
- Rice University
- And othres

Also given seminars in many industrial and academic organizations in Europe and Asia. Detailed list omitted.

GRANTS AND OTHER REVIEW FUNCTIONS

- Invited as National Science Foundation (NSF) grant review panels (many times)
- Invited as an external reviewer of a grant reviewer to NSF---equivalent organizations in other countries (Canada, England, Holland, France, etc.)
- Invited as a reviewer for tenure and other promotion reviewers for professors/scientists both in US and beyond.
- Invited as external Ph.D thesis examiners both within US and internationally (e.g. INRIA (France), Chamers University (Sweden), Tsinghua University (China), Chinese University of Science and Technology (China), Huazhong University of Science and Technology (China), etc.).

Section A: Teaching and Research Supervision

A.1: TEACHING

A series of new courses have been introduced and taught over years. The topics include:

1. Computer Architectures
2. Parallel Computer Architecture and Systems
3. Parallel and Functional Programming
4. Optimizing and Parallelizing Compilers
5. High-Performance Computing and Bioinformatics

A.2: RESEARCH SUPERVISION

Graduated students graduated under my supervision (A partial list):

The following Graduate students and Post---Docs have already completed their proposed research under my supervision:

PhD Level (a partial list):

1. Joshua Suetterlein
A Case for Asynchronous Many Task Runtimes: a Modeling approach for High

Summer 2017

2. Performance Computing and Big Data
3. Jaime Arteaga
Multigrain Parallelism: Bridging Coarse-Grain Parallel Programming And Fine-Grain Event-Driven Multithreading
Summer 2017
4. Kelly Livingston
Towards Co-Designed Energy Efficient Computing And Runtimes: Simulation-Framework And Experiments
2016
5. Sunil Shrestha
A framework for group locality aware multithreading
2015
6. Robert S. Pavel
Simulation Methodology and Tools for the Development of Novel Program Execution Models and Architectures
June 2015
7. Elkin Garcia
Toward High Performance and Energy Efficiency on Manycore Architectures
Summer 2014
8. Juergen Ributzka
Concurrency and Synchronization in the Modern Many---Core Era: Challenges and Opportunities
University of Delaware (USA), 2009 – 2013.
9. Daniel Orozco
TIDeFlow: A Dataflow---inspired execution model for high performance computing programs
University of Delaware (USA), 2007 – 2012.
10. Joseph B. Manzano
A comparison between virtual code management techniques
University of Delaware (USA), 2003 – 2011.
11. Ge Gan
Programming model and execution model for OpenMP on the Cyclops---64 manycore processor
University of Delaware (USA), 2004 – 2010.
12. Long Chen
Exploring novel many---core architectures for scientific computing
University of Delaware (USA), 2005 – 2010.
13. 1. Fei Chen
Enabling system validation for the many --- core supercomputer
University of Delaware (USA), 2001 – 2009.
14. Juan del Cuvillo
Breaking away from the OS shadow: A program execution model aware thread virtual machine for multicore architectures

University of Delaware (USA), 2001 – 2008.

15. Yuan Zhang

Static analyses and optimizations for parallel programs with synchronization

University of Delaware (USA), 2002 – 2008.

16. Mihailo Kaplarevic

Environmental genome informational utility system (EnGENIUS)

University of Delaware (USA), 2001 – 2007.

17. Weirong Zhu

Efficient synchronization for a large-scale multi-core chip architecture

University of Delaware (USA), 2002 – 2007.

18. Rishi Lee Khan

Engineering systems neuroscience: Modeling of a key adaptive brain control system involved in hypertension

University of Delaware (USA), 2000 – 2007.

19. Alban Douillet

A compiler framework for loop nest software-pipelining

University of Delaware (USA), 2001 – 2006.

20. Yanwei Niu

Parallelization and performance optimization of bioinformatics and biomedical applications targeted to advanced computer architectures

University of Delaware (USA), 2001 – 2005.

21. Robel Y. Kahsay

Advanced protein sequence analysis methods for structure and function prediction

University of Delaware (USA), 2001 – 2005.

22. Andres Marquez

The CARE architecture

University of Delaware (USA), 1995 – 2004.

23. Hongbo Yang

Power-aware compilation techniques for high performance processors

University of Delaware (USA), 1999 – 2003.

24. Parimala Thulasiraman

Irregular computations on fine-grain multithreaded architecture

University of Delaware (USA), 1995–2000.

25. Xinan Tang

Compiling for multithreaded architectures

University of Delaware (USA), 1995 – 1999.

26. Kevin Bryan Theobald

EARTH: An Efficient Architecture for Running Threads McGill University (Canada), 1990 – 1999.

27. Erik Richter Altman

Optimal software pipelining with function unit and register constraints

McGill University (Canada), 1991 – 1996.

28. Shashank Nemawarkar
Performance modeling and analysis of multithreaded architectures
McGill University (Canada), 1989 – 1996.
29. Vugranam C. Sreedhar
Efficient program analysis using DJ graphs
McGill University (Canada), 1990 – 1995.
30. Guy Tremblay
Parallel implementation of lazy functional languages using abstract demand propagation
McGill University (Canada), 1988 – 1994.
31. Qi Ning
Register allocation for optimal loop scheduling
McGill University (Canada), 1990 – 1993
32. Herbert H. J. Hum
The Super---Actor Machine: A hybrid dataflow/von Neumann architecture
McGill University (Canada), 1990 – 1992.
33. Robert Kim Yates
Semantics of timed dataflow networks
McGill University (Canada), 1988 – 1992.

MSLevel (a partial list, upto 2014):

1. Joshua Suetterlein
DARTS: A Runtime Based on the Codelet Execution Model
Spring 2014
2. Yao Wu
Memory Optimization in Codelet Execution Model on Many---Core Architectures
Spring 2014
3. Thomas St. John
Massively Parallel Breadth First Search Using a Tree---Structured Memory Model
University of Delaware (USA), 2007 – 2013.
4. Joshua Landwehr
Tapestry: Weaving Execution and Synchronization Models
University of Delaware (USA), 2009 – 2013.
5. Sunil Shrestha
Parallel Low---Overhead Data Collection Framework for a Resource Centric Performance Analysis Tool
University of Delaware (USA), 2007 – 2012.
6. Xiaomi An
Memory State Flow Analysis and Its Application
University of Delaware (USA), 2009 – 2011.
7. Juergen Ributzka
Toward a software pipelining framework for many---core chips

- University of Delaware (USA), 2005 – 2009.
8. Jonathan L. Barton
Hardware implementation of a synchronization state buffer in VHDL
University of Delaware (USA), 2005 – 2008.
 9. Mark Pellegrini
A case study of the Mstack cross---platform benchmark on the Cray MTA---2
University of Delaware (USA), 2004 – 2008.
 10. Matthew Wells
University of Delaware (USA), 2006 --- 2008.
 11. Yi Jiang
Design and implementation of tool---chain framework to support OpenMP single source compilation on cell platform
University of Delaware (USA), 2006 – 2008.
 12. Long Chen
Optimizing the Fast Fourier Transform on a many---core architecture
University of Delaware (USA), 2005 – 2008.
 13. Liping Xue
Efficient mapping of fast Fourier transform on the Cyclops---64 multithreaded architecture
University of Delaware (USA), 2005 – 2007.
 14. Ge Gan
CDP: A multithreaded implementation of a network communication protocol on the Cyclops---64 multithreaded architecture
University of Delaware (USA), 2004 – 2007.
 15. Eun Jung Park
Methodology of dynamic compiler option selection based on static program analysis: Implementation and evaluation
University of Delaware (USA), 2004 – 2007.
 16. Dimitrij Krepis
A study of simulation and verification of a many---core architecture on two modern reconfigurable platforms
University of Delaware (USA), 2004 – 2007.
 17. Divya Parthasarathi
Tower methodology for verification of multi---core architecture: A case study
University of Delaware (USA), 2003 – 2005.
 18. Ying Ping Zhang
A study of architecture and performance of IBM Cyclops64 interconnection network
University of Delaware (USA), 2003 – 2005.
 19. Vishal Karna
Multiprocessor SOC Verification
University of Delaware (USA), 2002 – 2005.
 20. Robert Klosiewics

A Parallel Debugger for the Cyclops Architecture
University of Delaware (USA), 2002 – 2004

21. Inanc Dogru
An integer linear programming approach to reduce register spills on itanium processors
University of Delaware (USA), 2002 – 2004.
22. Xing Wang
Quantitive Study of Human---Computer interaction in adaptive search on Mobile Handsets and its
Localization for Mandarin Chinesse
University of Delaware (USA), 2001 – 2004.
23. Weirong Zhu
Multithreaded Parallel Implementation of HPMPFAM on EARTH
University of Delaware (USA), 2001 – 2004.
24. Fei Chen
Implementing Parallel CG Algorithm on the EARTH Multithreaded Architecture
University of Delaware (USA), 2001 – 2004.
25. Yan Xie
Code Size Oriented Memory Allocation for Temporary Variables University of Delaware (USA), 2001
– 2003.
26. Chuan Shen
A Portable Runtime System and its Derivation for the Hardware SU Implementation
University of Delaware (USA), 2001 – 2003.
27. Kapil Khosla
Binary Diffing
University of Delaware (USA), 2001 – 2003.
28. Tamal Basu
Survivability of routing protocols in large scale clustered fractal networks
University of Delaware (USA), 2001.
29. Rishi Kumar
Efficient Parallelization of Reductions and Loop Based Programs on EARTH
University of Delaware (USA), 1999 – 2001.
30. Praveen Thiagarajan
A Visual Perspective to Motif/Pattern Analysis
University of Delaware (USA), 1999 – 2001.
31. Juan. Del. Cuvillo
Whole Genome Comparison Using A Multithreaded Parallel Implementation
University of Delaware (USA), 1999 – 2001.
32. Christopher J. Morrone
A EARTH Runtime System For Multi---Processor/Multi---Node Beowulf Cluster
University of Delaware (USA), 1999 – 2001.
33. Alban Douillet
Register Stack and Optimal Allocation Instruction Placement

University of Delaware (USA), 1999 – 2001.

34. Sean Ryan
Developing a software distributed shared memory for the EARTH platform
University of Delaware (USA), 1999 – 2000.
35. Kamala Prasad Kakulavarapu
Dynamic load balancing issues in the EARTH runtime system
McGill University (Canada), 1996 – 2000.
36. Ian Stuart MacKenzie Walker
Towards a Custom EARTH Synchronization Unit University of Delaware (USA), 1998 – 1999.
37. Cheng Li
Earth---SMP: multithreading support on an SMP cluster
University of Delaware (USA), 1997 – 1999.
38. Lei Liu
The effect of resource complexity on modulo scheduling
University of Delaware (USA), 1997 – 1999.
39. Maria---Dana Tarlescu
The elastic history buffer: A multi---hybrid branch prediction scheme using static classification
McGill University (Canada), 1996 – 1999.
40. Dionis Hristov
Development of tests for the ATM signaling protocol
McGill University (Canada), 1998.
41. Hisham Johnathon Petry
Comparison of SC derived memory models and location consistency on shared memory architectures
McGill University (Canada), 1995 – 1997.
42. Haiying Cai
Dynamic load balancing on the EARTH---SP system
McGill University (Canada), 1997.
43. Raul Esteban Silvera---Munoz
Static instruction scheduling for dynamic issue processors
McGill University (Canada), 1996 – 1997.
44. Shaohua Han
Implementation of nested relations in a database programming language
McGill University (Canada), 1996 – 1997.
45. Hongru Cai
McGill University (Canada), 1995 – 1997.
46. Artour V Stoutchinin
Optimal software pipelining: Integer linear programming approach
McGill University (Canada), 1994 – 1996.
47. Shamir Fatehali Merali

- Designing and implementing memory consistency models for shared-memory multiprocessors
McGill University (Canada), 1993 – 1996.
- 48.** Alberto Jimenez
McGill University (Canada), 1993 – 1996.
- 49.** Nasser Elmasri
TCL: Experiences on a multiprocessor with dual-processor nodes
McGill University (Canada), 1992 – 1995.
- 50.** Renhua Wen
The design and implementation of an accurate array data-flow analyzer in the HPC compiler
McGill University (Canada), 1993 – 1995.
- 51.** Luis Alfonso Lozano
Exploiting short-lived variables in superscalar processors
McGill University (Canada), 1992 – 1994.
- 52.** Chandrika Mukerji
Register allocation using cyclic interval graphs
McGill University (Canada), 1991 – 1994.
- 53.** M Ravi Shanker
A parallel implementation of the A*-Viterbi algorithm for speech recognition
McGill University (Canada), 1991 – 1993.
- 54.** Cecile Moura (1991 – 1993)
SuperDLX – A Generic Superscalar Simulator
McGill University (Canada), 1991 – 1993.
- 55.** Qi Ning
Register allocation for optimal loop scheduling
McGill University (Canada), 1991 – 1993.
- 56.** Russell Olsen
Collective Loop Fusion for Array Contraction
McGill University (Canada), 1989 – 1992.
- 57.** Nematollah Shiri-Varnaamkhaasti
A design and implementation of unimodular transformations of loops
McGill University (Canada), 1990 – 1992.
- 58.** Yue-Bong Wong
A petri-net model for loop scheduling
McGill University (Canada), 1989 – 1991.
- 59.** Jean-Marc Monti
Interprocessor communication supports for a multiprocessor dataflow machine
McGill University (Canada), 1989 – 1991.
- 60.** Alan Emtage
McGill University (Canada), 1988 – 1991.
- 61.** Zaharias Paraskevas



CAPSL
Computer Architecture and Parallel Systems Laboratory
Department of Electrical and Computer Engineering

Code generation for dataflow software pipelining
McGill University (Canada), 1987 – 1989.

Postdoc (a partial list):

1. Stephane Zuckerman (2011-2016)
2. Long Zheng (2012-2013)
3. Tu Hao (2012-2013)
4. Chen Chen (2011– 2013).
5. Souad Koliai (2012– 2013).
6. Xiaoxuan Meng (2009 – 2011).
7. Handong Ye (2008 – 2009).
8. Yeonseok Lee (2007 – 2008).
9. Jean Christophe Beyler (2007 – 2008).
10. Ziang Hu (1999 – 2008).
11. Haiping Wu (2000 – 2008).
12. Ioannis E. Venetis (2006 – 2007).
13. Shuxin Yang (2005 – 2007).
14. Ted T. Jeong (2005 – 2006).
15. Hongbo Rong (2001 – 2005).
16. Hirofumi sakane (2001 – 2005).
17. Andres Marquez (2004).
18. Jozsef bukszar (2002 – 2004).
19. Jizhu Lu (2000 – 2004).
20. Jianshan Tang (2002 – 2003).
21. Rongcai Zhao (2000 – 2001).
22. José N. Amaral (1998 – 2000).
23. Ruppa Thulasiraman (1998 – 2000).
24. Gerd Heber (1997 – 1999).
25. Chihong Zhang (1998 – 1999).
26. Olivier Maquelin (1994 – 1998).
27. Jian Wang (1995 – 1997).
28. Xinmin Tian (1993 – 1996).
29. Benoit Dupont Dinechi (1995 – 1996).
30. Ramaswamy Govindarajan (1990 – 1994).
31. Guoning Liao (1991 – 1993).

Those who have graduated are trained in the field of parallel architectures and compilers, and their generally have been successful in their career as evidenced by the fact that they have been working (or worked) as tenure-track university professors or as engineers in key industrial sectors.

Section B: Scholarship

LIST OF RESEARCH PUBLICATIONS (partial list)

The contributions are listed under the following category:

Referred Journal Publications
Referred Conference
Publications Books/ Book
Chapters/ Notes Sets Patents

A. Referred Journal Publications (partial list)

1. Peng Qu, Jin Yan, You-Hui Zhang, Guang R Gao. Parallel Turing Machine, a Proposal. Journal of Computer Science and Technology. Volume 32, Issue 2, Pages 269-285
2. Yao Wu, Long Zheng, Brian Heilig, Guang R Gao. HAMR: A dataflow-based real-time in-memory cluster computing engine. International Journal of High Performance Computing Applications.
3. Daniel Orozco, Elkin Garcia, Robert Pavel, Jaime Arteaga, Guang Gao. The Design and Implementation of TIDeFlow: A Dataflow-Inspired Execution Model for Parallel Loops and Task Pipelining. International Journal of Parallel Programming. Volume 44, Issue 2, Pages 278-307
4. Roberto Giorgi, Rosa M. Badia, François Bodin, Albert Cohen, Paraskevas Evripidou, Paolo Faraboschi, Bernhard Fechner, Guang R. Gao, Arne Garbade, Rahul Gayatri, Sylvain Girbal, Daniel Goodman, Behran Khan, Souad Koliaï, Joshua Landwehr, Nhat Minh LêFeng Li, Mikel Lujà Avi Mendelson, Laurent Morin, Nacho Navarro, Tomasz Patejko, Antoniu Pop, Pedro Trancoso, Theo Ungerer, Ian Watson, Sebastian Weis, Stéane Zuckerman, Mateo Valero, TERAFLUX: Harnessing dataflow in next generation teradevices, Microprocessors and Microsystems --- Journal, Available online 18 April 2014, ISSN 0141---9331.
5. Chen Chen, Souad Koliai and Guang R. Gao. Exploitation of Locality for Energy Efficiency for Breadth First Search in Fine---grain Execution Models. Tsinghua Science and Technology --- Journal, Volume 18, Number 3, June 2013.
6. Haitao Wei, Mingkang Qin, Junqing Yu, Dongrui Fan and Guang R. Gao. StreamTMC: Stream Compilation for Tiled Multi---core Architectures. Elsevier Journal of Parallel and Distributed Computing (JPDC), Volume 73, Issue 4, April 2013, Pages 484-494.
7. Haitao Wei, Junqing Yu, Huafei Yu, Mingkang Qin, Guang R. Gao. Software Pipelining for Stream Programs on Resource Constrained Multicore Architectures. IEEE Transactions on Parallel and Distributed Systems, Volume 23(12), 2338---2350, Dec. 2012.
8. Daniel Orozco, Elkin Garcia, Rishi Khan, Kelly Livingston and Guang R. Gao. Toward High Throughput Algorithms on Many Core Architectures. ACM Transactions on Architecture and Code Optimization (TACO), Volume 8, Issue 4, January 2012, Article No. 49.

9. Jack B. Dennis, Guang R. Gao, Xiao X. Meng. Experiments with the Fresh Breeze tree-based memory model, *Computer Science --- Research and Development*, Volume 26 Issue 3---4, pp. 325--- 337, June 2011.
10. Guangming Tan, Vugranam C. Sreedhar and Guang R. Gao. Analysis and Performance Results of Computing Betweenness Centrality on IBM Cyclops64, *Journal of Supercomputing*. Vol. 56 Issue 1, April 2011.
11. Guangming Tan, Ninghui Sun and Guang R. Gao. Improving Performance of Dynamic Programming via Parallelism and Locality on Multi-core Architectures, *IEEE Transactions on Parallel and Distributed Systems*, Vol.20, No.2, 2009, pp. 261---274.
12. Hongbo Rong, Alban Douillet, Guang R. Gao. Register allocation for software pipelined multidimensional loops. *ACM Trans. Program. Lang. Syst.* 30(4), July 2008.
13. M. Kaplarevic, A.E. Murray, G. Gao, EnGENIUS --- Environmental Genome Informational Utility System, *Journal of Bioinformatics and Computational Biology*, JBCB---119R1, July, 2008.
14. Rishi L. Khan, Rajanikanth Vadigepalli, Mary K. McDonald, Robert F. Rogers, Guang R. Gao and James S. Schwaber, Dynamic transcriptomic response to acute hypertension in the nucleus tractus solitaries, *AJP --- Regulatory, Integrative and Comparative Physiology*. Volume 295: R15---R27, July, 2008.
15. Hongbo Rong, Zhizhong Tang, R. Govindarajan, and Alban Douillet, Guang R. Gao, Single--dimension software pipelining for multi--dimensional loops. *ACM Transactions on Architecture and Code Optimization*, Vol.4, No.1, January, 2007.
16. Weirong Zhu, Yanwei Niu, and Guang R. Gao, Performance Portability on EARTH: A Case Study across Several Parallel Architectures, *Cluster Computing*, Volume 10, Number 2, Page 115---126, 2007.
17. Rishi L Khan, Gregory E Gonye, Guang Gao and James S Schwaber, A universal reference sample derived from clone vector for improved detection of differential gene expression, *BMC Genomics*, Volume 7:109, May, 2006.
18. Haiping Wu, Ziang Hu, Joseph Manzano and Guang. R. Gao, Madd Operation Aware Redundancy Elimination, *International Journal of Software Engineering and Knowledge Engineering*, Vol. 15, No. 2, Pages: 357---362, 2005
19. Hongbo Yang, R. Govindarajan, Guang R. Gao, ZiangHu, Improving Power Efficiency with Compiler--Assisted Cache Replacement, *Journal of Embedded Computing*, Vol. 1, No. 4, Pages: 487---499, 2005.
20. Robel Kahsay, Li Liao , Guang Gao, An Improved Hidden Markov Model for Transmembrane Protein Topology Prediction and Its Applications to Complete Genomes, *Bioinformatics*, Volume 21, Number 9, Pages: 1853---158, 2005.
21. Robel Kahsay, Guoli Wang, Guang Gao, Li Liao and Roland Dunbrack, Quasi---Consensus Based COMParison of Profile Hidden Markov Models for Protein Sequences, *Bioinformatics*, Volume 21, Number 10, Pages: 2287---2293, 2005
22. Weirong Zhu, Yanwei Niu, Jizhu Lu, Chuan Shen and Guang R. Gao, A Cluster---Based Solution for High Performance Hmmpfam Using EARTH Execution Model, *International Journal of High Performance Computing and Networking*, Vol 2, Issue 2/3/4, 2004.
23. Parimala Thulasiraman, Kevin B. Theobald, Ashfaq A. Khokhar, and Guang R. Gao, Efficient Multithreaded Algorithms for the Fast Fourier Transform, *Parallel and Distributed Computing Practices*, Vol. 5, No. 2, Pages: 177---191, 2004.

24. Parimala Thulasiraman, Ashfaq A. Khokhar, Gerd Heber, Guang R. Gao, A Fine-Grain Load Adaptive Algorithm of the 2D Discrete Wavelet Transform for Multithreaded Architectures, *Journal of Parallel and Distributed Computing (JPDC)*, Vol.64, No.1, Pages: 68-78, January 2004.
25. Dong Rui Fan, Hongbo Yang, Gaung R. Gao, and Rong Cai Zhao, Evaluation and Choice of Various Branch Predictors for Low-Power Embedded Processor, *Journal of Computer Science and Technology*, Vol. 18, No. 6, Pages: 833-838, November, 2003.
26. Guy Tremblay, Christopher J. Morrone, José N. Amaral, and Guang R. Gao, Implementation of the EARTH Programming Model on SMP Clusters: a Multi-Threaded Language and Runtime System, *Concurrency and Computation: Practice and Experience*, Vol. 15, No. 9, Pages: 821-844, August 2003.
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C. Patents (partial list)

1. Title: Codeletset Representation, Manipulation, and Execution---Methods, System And Apparatus Rishi Khan, Daniel Orozco, Guang Gao, Kelly Livingston.
Patent number:
2012067688 Date of Patent:
May 25 2012.
2. Title: Runspace method, system and apparatus Rishi Khan, Daniel Orozco, Guang R. Gao. Patent No. US 2011/0246823 A1

Date of Patent: Oct. 6, 2011

3. Title: Task---Oriented Node---Centric Checkpointing (TONCC) Rishi Khan, Guang R. Gao, Apperson H. Jhonson
 Patent No. US 2011/0246823 A1
 Date of Patent: Oct. 6, 2011
4. Title: Systems and Methods for Logic Verification Guang R. Gao, Fei Chen
 Patent No. US 7.934.179 B2
 Date of Patent: April 26, 2011
5. Title: Methods and Products for Processing Loop Nests Hongbo Rong, Guang R. Gao, Alban Douillet, R. Govindarajan Patent No. US 7.631.305 B2
 Date of Patent: Dec. 8, 2009
6. Title: Data driven logic simulation chip and tool chain Fei Chen, Guang R. Gao
 Patent No. US 2009/0222252 A1
 Date of Patent: Sep 3, 2009
7. Title: Methods and Apparatus for emulation of logic circuits Hirofumi Sakane, Levent Yakay, Vishal Karma, Clement Leung, Guang R. Gao.
 Patent No. US 7.356.454 B2
 Date of Patent: April 8, 2008
8. Title: Method for Integrating Software Pipelining with Multithreading Guang R. Gao, with Hongbo Rong, Alban Douillet, R. Govindarajan Provisional Application No.: 60/507,043
 Filing Date: Sept. 29, 2003
 US patent application
 pending
9. Title: Method and Apparatus for Real---Time Multithreading Guang R. Gao and Kevin Theobald
 Patent No. US 2005/0188177 A1
 Date of Patent: Aug. 25, 2005
10. Title: Method And Apparatus For Iterative Emulation Of Large Logic Circuits Containing Multiple Identical Logic Modules
 Guang R. Gao, with Hirofumi Sakane, Levent Yakay, Vishal Karna, Clement Leung
 Provisional Application No.: 60/512,376
 Filed Date: November 17, 2003
 US patent application pending

B.3: CONTRACTS AND GRANTS

Gao has been a PI or Co-PI of may research projects with government sponsors (DoD, DOE, NSF,

NIH, NASA, etc.), state government, industry, etc. The list is omitted.

Section C: Services

C.1: UNIVERSITY ACTIVITIES AND SERVICES (involved)

- Member, Undergraduate award Committee
- Member, Faculty Strategic Planning Committee, ECE Dept.
- Member, Faculty Recruit Committee
- Chair, Secondary Appointment Committee, ECE Dept.
- Member, Department recruiting committee
- Member, Secondary Appointment Committee
- Participating faculty retreat meeting
- Dean's ad hoc group for supercomputing
- Participant Engineering Outreach program
- Advisor in the university Undergraduate Research Opportunity program.
- Chairing the departmental Committee on Promotion & Tenure
- College Election Committee
- Dean search committee.
- Graduate study and PhD exam revision committee
- Ad Committee of Educational in Bioinformatics.
- DBI Scientific Committee.
- ICRSS committee (Instructional, Computing and Research Support Services Committee).