University of Delaware
Department of Electrical and Computer Engineering
ELEG652 - Principles of Parallel Architectures
Fall 2014
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Assignment 4
Memory Models and Cache Consistency

Due on Saturday Nov. 1st, 23:59

Memory Models

1. [50%] For this part of the homework, you will study the effect that different memory models have on parallel programs

   a) [10%] Explain Sequential Consistency.

   b) [10%] Explain Coherence Consistency, Weak Consistency and Release Consistency.

   c) [10%] Explain how do these memory models in b) relax the order compared with sequential consistency and what are the potential performance optimization opportunities?

   d) [20%] For the following, please list all possible values for R1 and R2 at the end of execution. X, R1and R2 are initially equal to 0.

i. Sequential Consistency	
Thread 0	Thread 1
X=X+1 R1 = X	R2 = X X=3
ii. Weak Consistency	
Thread 0	Thread 1
X=X+1 R1 = X	R2 = X X=3
iii. Weak Consistency	
Thread 0	Thread 1
X=X+1 SYNC R1 = X	R2 = X SYNC X=3

Cache Coherency Protocols

2. [50%] A multiprocessor system is executing the following code:

Processor 1	Processor 2

LD R1, _a
MUL R6, R1, R1
ADD R1, R1, 1
ST R1, _a
INC R3
LD R7, _a
	MOV R2, 5
	ST R2, _a
	INC R2
	INC R2
	LD R6, _a
	MUL R2, R2, R6
	ST R2, _a

- All loads and stores have no delay, so they execute in one cycle each
- Processor 1 and 2 execute instructions at the same frequency with no interruption from the OS or other programs. Thus, instructions in processor 1 will execute in the same cycle as processor 2. For example, the load instruction from processor 1 will execute at the same time as the move instruction from Processor 2, and all of this will occur during cycle 1.
- Operations in registers do not change the state of the cache. Only loads and stores can do that.
- All operations are considered atomic with respect to each other
- All cache lines and blocks are initially in the invalid state (I).

In the following table, the **Status** column is the state of the cache line housing the variable AFTER the current instruction has finished. The **Data Supplied By** column tells us who will supply the data, P1'cache, P2'cache or Memory for maintaining the protocols.

a) [25%] Please fill out the *Status* and *Data Supplied By* columns assuming a cache using the MSI protocol.

	P1			P2			
Cycle	Cache	Status	OP	Cache	Status	OP	Data Supplied by
1	_a		load	N/A		mov	
2	_a		mul	_a		store	
3	_a		add	_a		increment	
4	_a		store	_a		increment	
5	_a		increment	_a		load	
6	_a		load	_a		mul	
7	_a		N/A	_a		store	

b) [25%] Please fill out the *Status* and *Data Supplied By* columns assuming a cache using the MESI protocol.

	P1			P2			
Cycle	Cache	Status	OP	Cache	Status	OP	Data Supplied by
1	_a		load	N/A		mov	
2	_a		mul	_a		store	
3	_a		add	_a		increment	
4	_a		store	_a		increment	
5	_a		increment	_a		load	
6	_a		load	_a		mul	
7	_a		N/A	_a		store	

Submission:

Submit a report with your answers using an IEEE Paper Template for the report (http://www.ieee.org/conferences_events/conferences/publishing/templates.html). Remember to cite all your sources.

Include any source files you wrote. Each program you write must be commented and have its own Makefile.

Remember to include the HW/SW specifications of the machine(s) where you run your experiments.

Send all the files as a single ZIP named *<YOUR_NAME>-lab<NUMBER_OF_LAB>-eleg652-14f.zip* (e.g. *johndoe-lab1-eleg652-14f.zip*) to Jaime Arteaga jaime@udel.edu with subject *ELEG652-14F LAB4* before the specified deadline.

If you miss the deadline, you can submit the homework until 17.45 of the following Tuesday, with the homework's total grade being decreased by 10% per day (i.e. homework will be graded over 100% until 23.59 of Friday, 90% until 23.59 of Saturday, 80% until 23.59 of Sunday, 70% until 23.59 of Monday, 60% until 17.45 of Tuesday).