

University of Delaware  
Department of Electrical and Computer Engineering  
**ELEG652 - Principles of Parallel Architectures**  
Fall 2014  
*Prof. Guang R. Gao*

**Assignment 5**  
***Dataflow***

**Due on Monday Nov. 24<sup>th</sup>, 23:59**

1. [50%] Show the pushing and flow of tokens in the Conditional Expression in slide 36 of Dataflow Part1 slides. You are free to define p, f, and g functions.
2. [50%] Show the pushing and flow of tokens in the Loop Schema in slide 38 of Dataflow Part1 slides for four iterations. You are free to define the loop operation and the condition. The initial state of this graph has a token FALSE in the arc labeled with F.

***Please provide your answers in form of power point slides so the motion of tokens is easier to create and see.***

***Submission:***

Submit a report with your answers using an IEEE Paper Template for the report ([http://www.ieee.org/conferences\\_events/conferences/publishing/templates.html](http://www.ieee.org/conferences_events/conferences/publishing/templates.html)). Remember to cite all your sources.

Include any source files you wrote. Each program you write must be commented and have its own Makefile.

Remember to include the HW/SW specifications of the machine(s) where you run your experiments.

Send all the files as a single ZIP named <YOUR\_NAME>-lab<NUMBER\_OF\_LAB>-eleg652-14f.zip (e.g. johndoe-lab1-eleg652-14f.zip) to Jaime Arteaga [jaime@udel.edu](mailto:jaime@udel.edu) with subject ELEG652-14F LAB5 before the specified deadline.

If you miss the deadline, you can submit the homework until 17.45 of the following Tuesday, with the homework's total grade being decreased by 10% per day (i.e. homework will be graded over 100% until 23.59 of Friday, 90% until 23.59 of Saturday, 80% until 23.59 of Sunday, 70% until 23.59 of Monday, 60% until 17.45 of Tuesday).