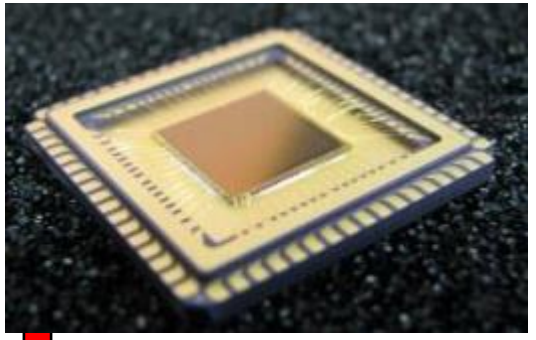
How to Build an LED Projector

SLEDS Project Organization Overview

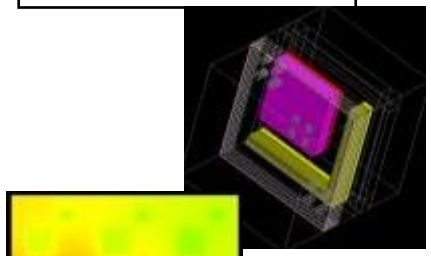
Design/Grow SLEDS (UIowa & Teledyne)

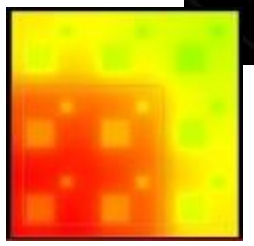
Test/Optimize discrete SLEDS devices (U Iowa)

Develop CMOS Drivers & Process, Package, Test Arrays (U Delaware)



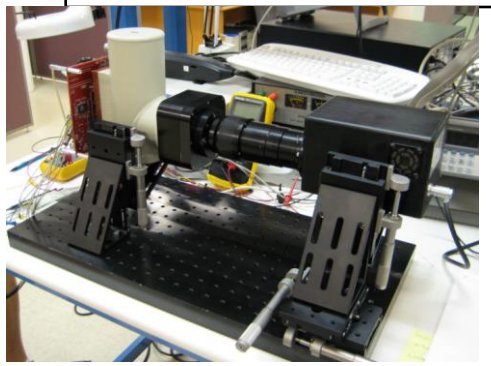
Develop Thermal Models for Array (ATEC)





Test SLEDS Arrays

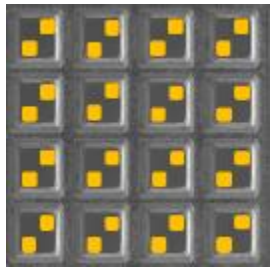
(Nova Sensors)

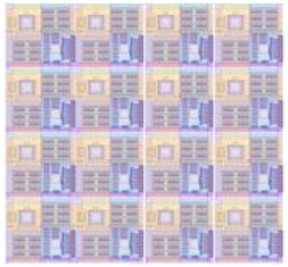


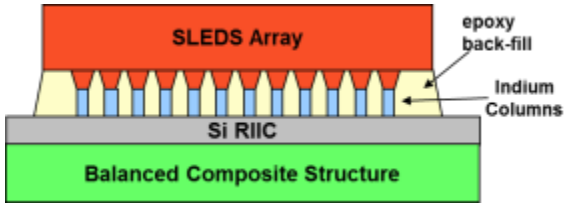
(KHILS)

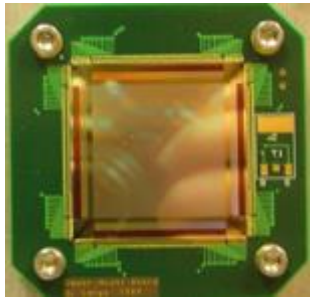
SLEDS System Description Part 1

Emitter Array + Silicon RIIC → Hybrid Array → Packaged 512x512 Array



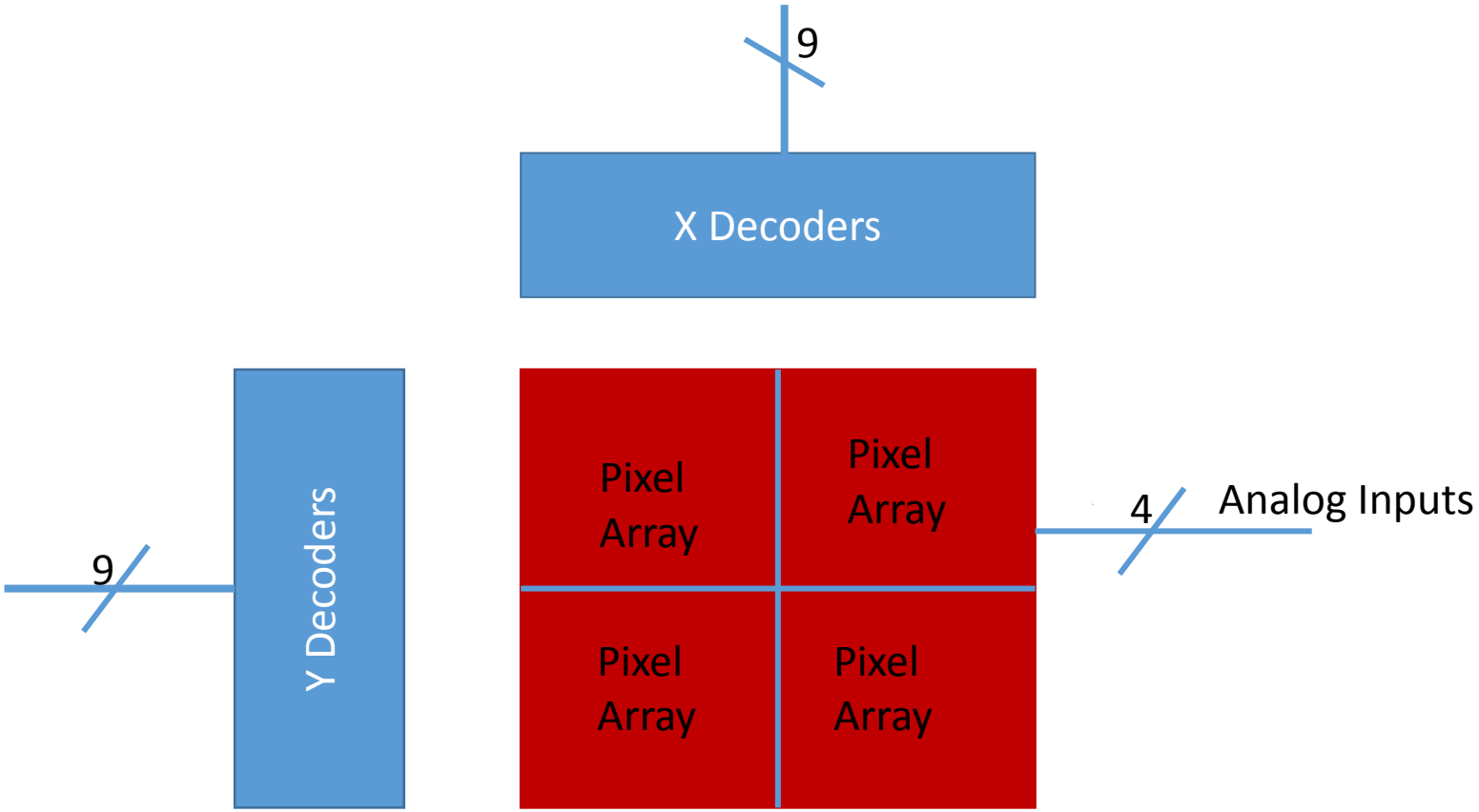






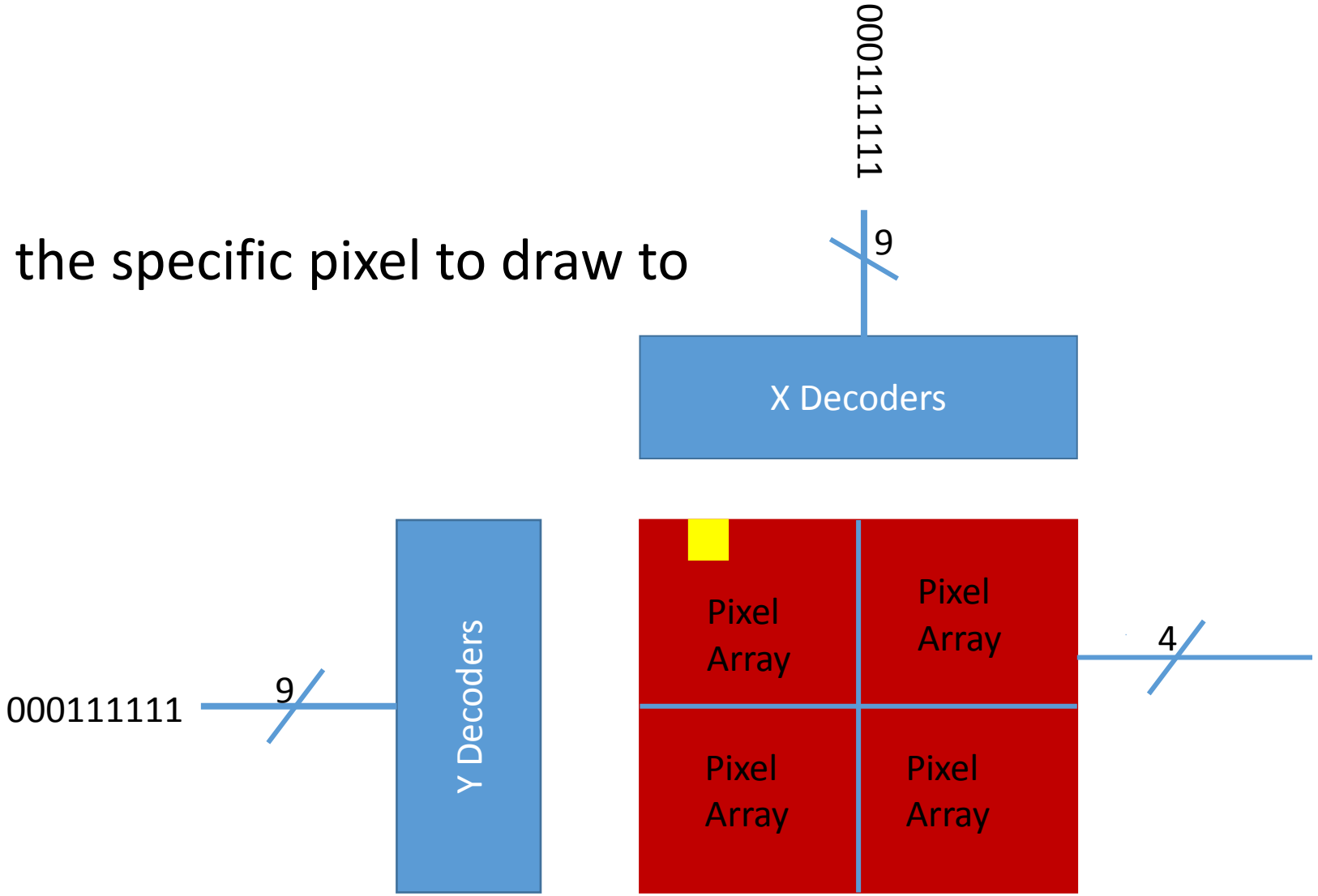
- 512x512, 48µm-pitch, 1-color MWIR SLEDS array
- Packaged in liquid nitrogen Dewar connected to CSE and tested at KHILS
- Semiconductor-based SLEDS are capable of higher apparent temperatures & frame rates compared to TPAs, enabling emulation of hot, highly dynamic scenes

Read In Integrated Circuit (RIIC) Overview

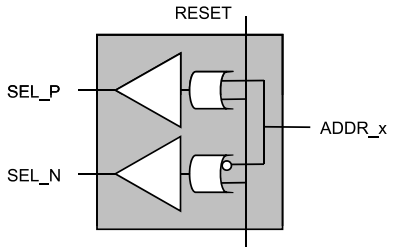


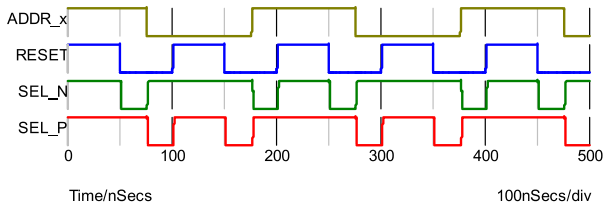
Decoders

- Used to select the specific pixel to draw to
- Domino logic



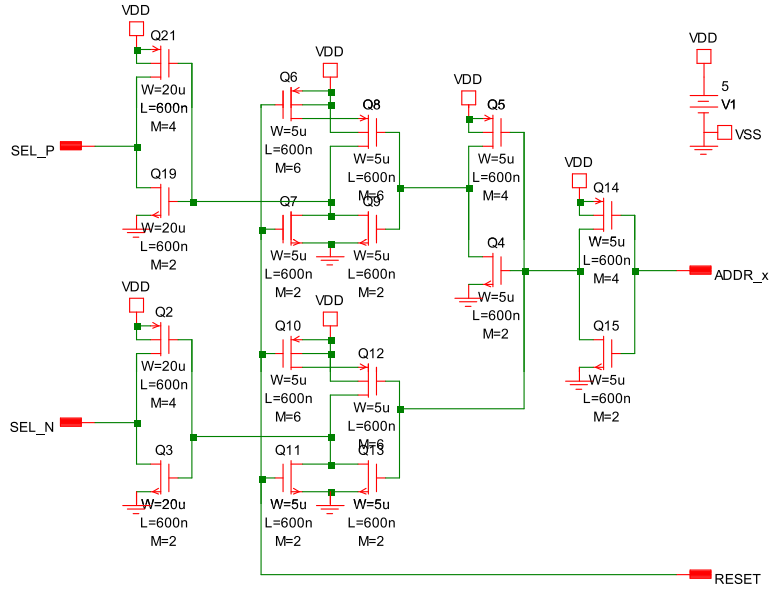
Driver Circuits



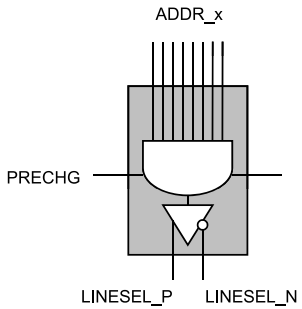


Decoder Driver Cell

ADDR_x	RESET	SEL_P	SEL_N
0	0	0	1
1	0	1	0
X	1	**1**	**1**



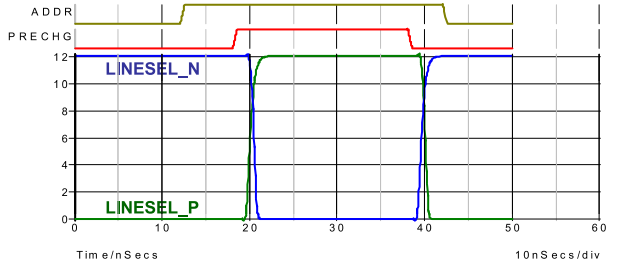
Domino Logic Decoders

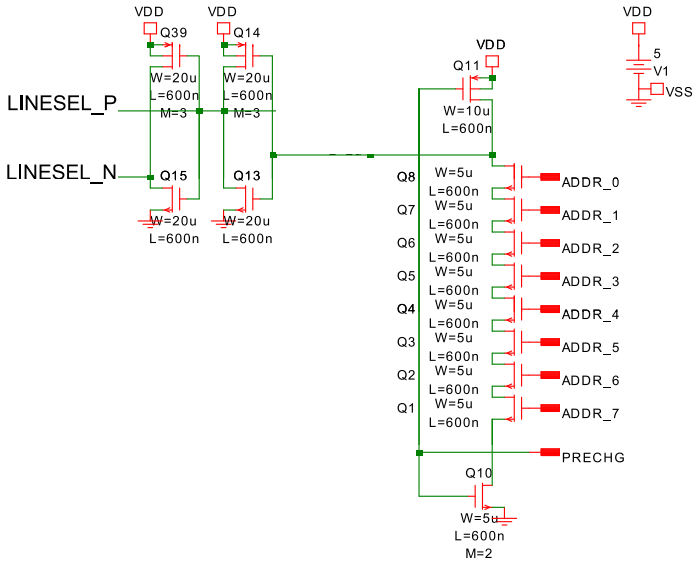


Note: LINESEL_P connects to X,Y and LINESEL_N connects to X_BAR, Y_BAR.

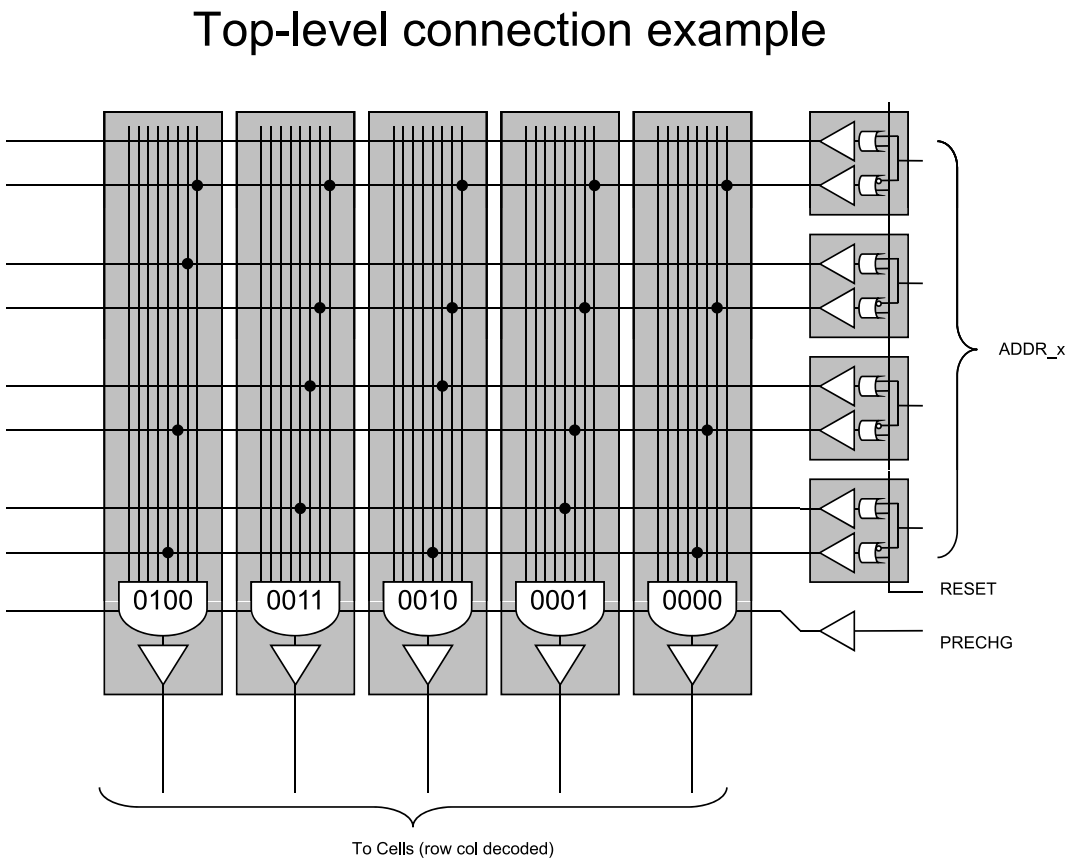
Row/Col Decoder Cell

ADDR_x	PRECHG	LINESEL_P	LINESEL_N
X	0	0	1
0	1	0	1
1	1	**1**	**0**

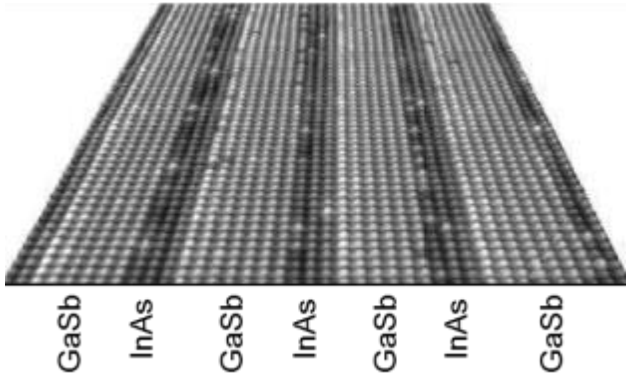




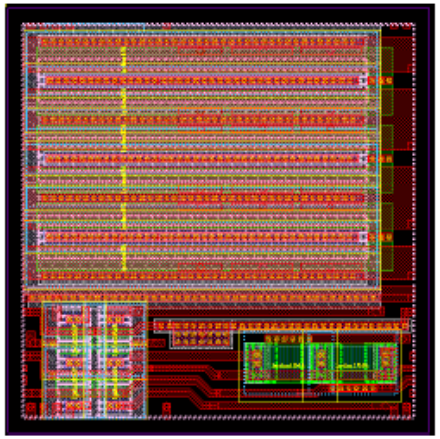
Combined Driver and Decoder Circuits



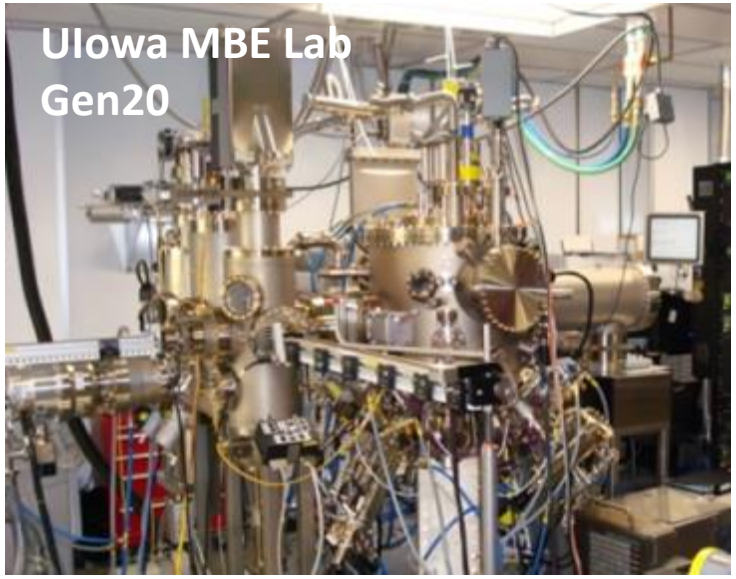
Emitter Array and CMOS Pixel



STM Cross Sectional Image of InAs/GaSb SLEDS Superlattice

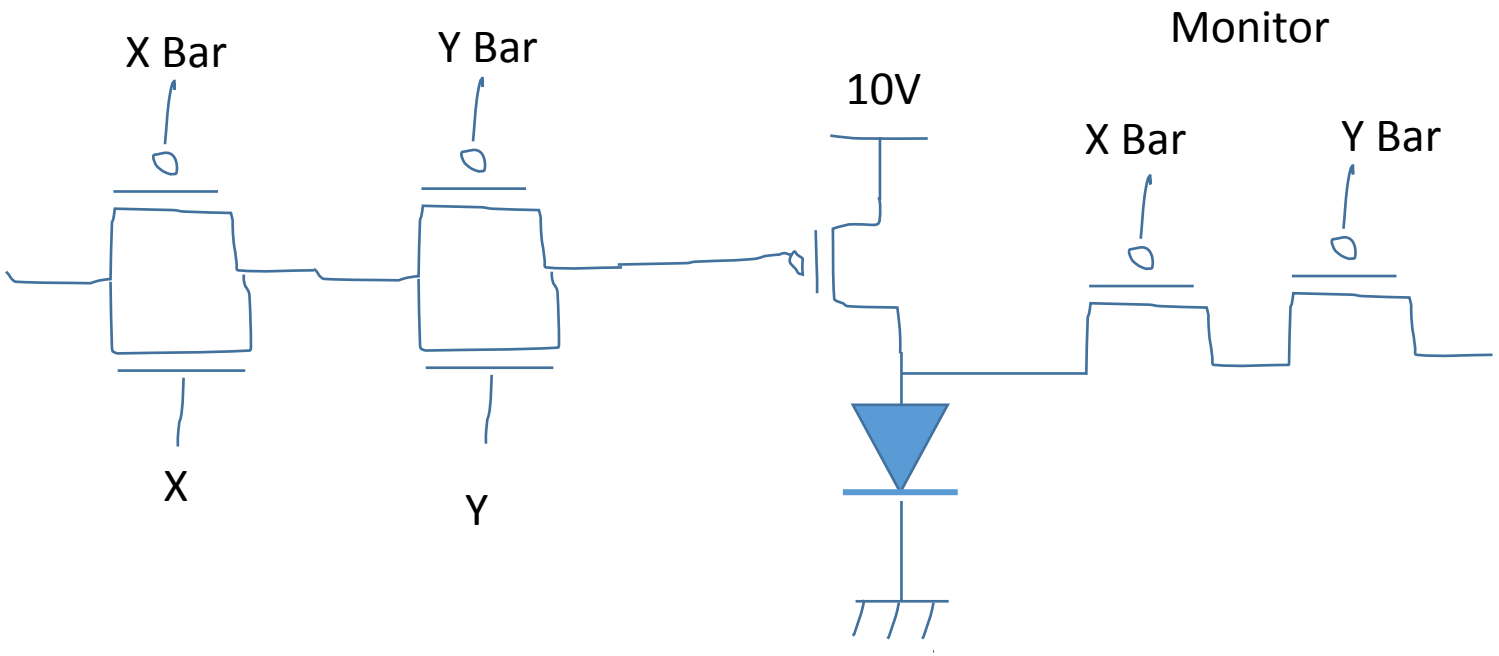


RIIC Single Pixel Layout



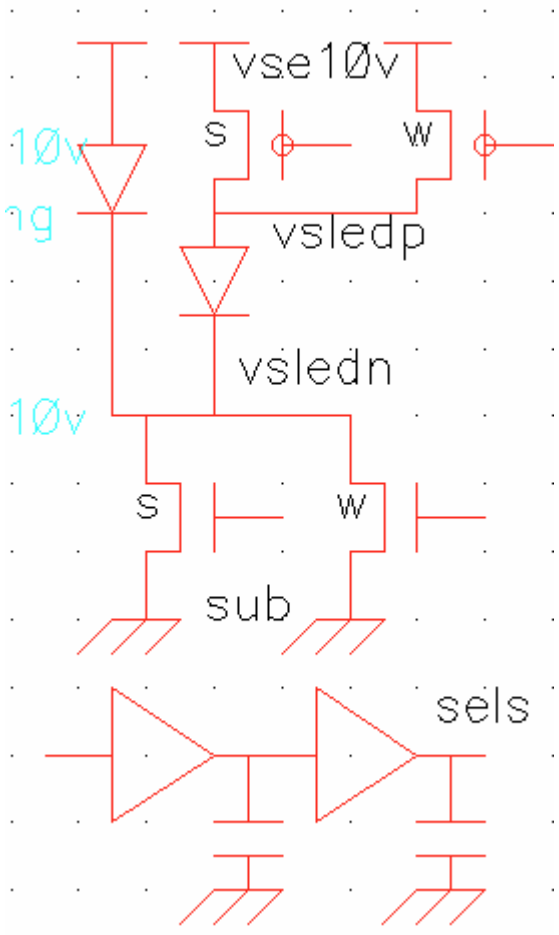
- SLEDS
  - Fabricated using nanostructured InAs/GaSb superlattices, requiring precision growth by Molecular Beam Epitaxy (MBE)
- RIIC
  - Designed to provide current and voltage swings required by SLEDS
- Close Support Electronics (CSE)
  - Must provide 1kHz frame rate for SLEDS IRSP

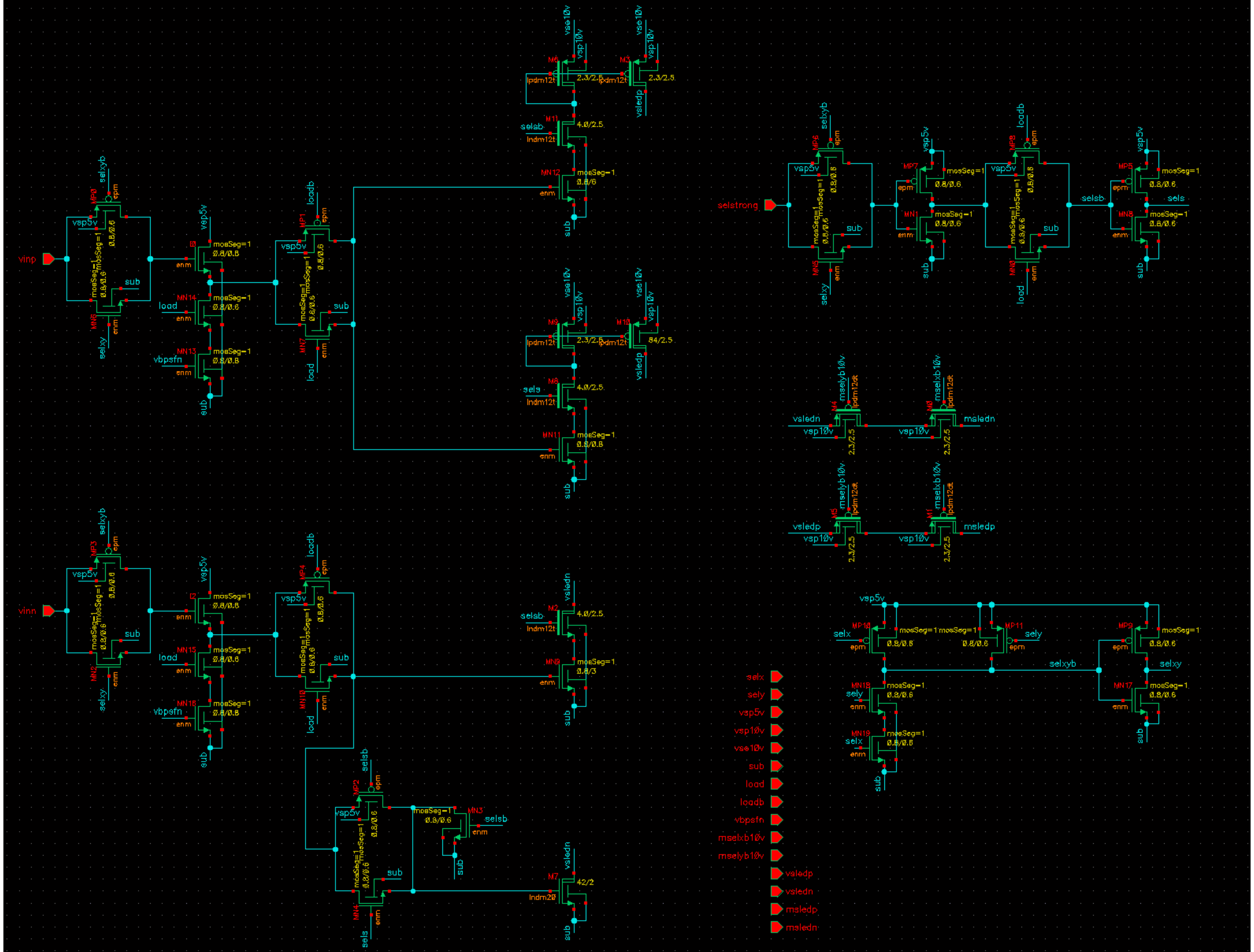
Original Pixel Circuit



CMOS Pixel Advances

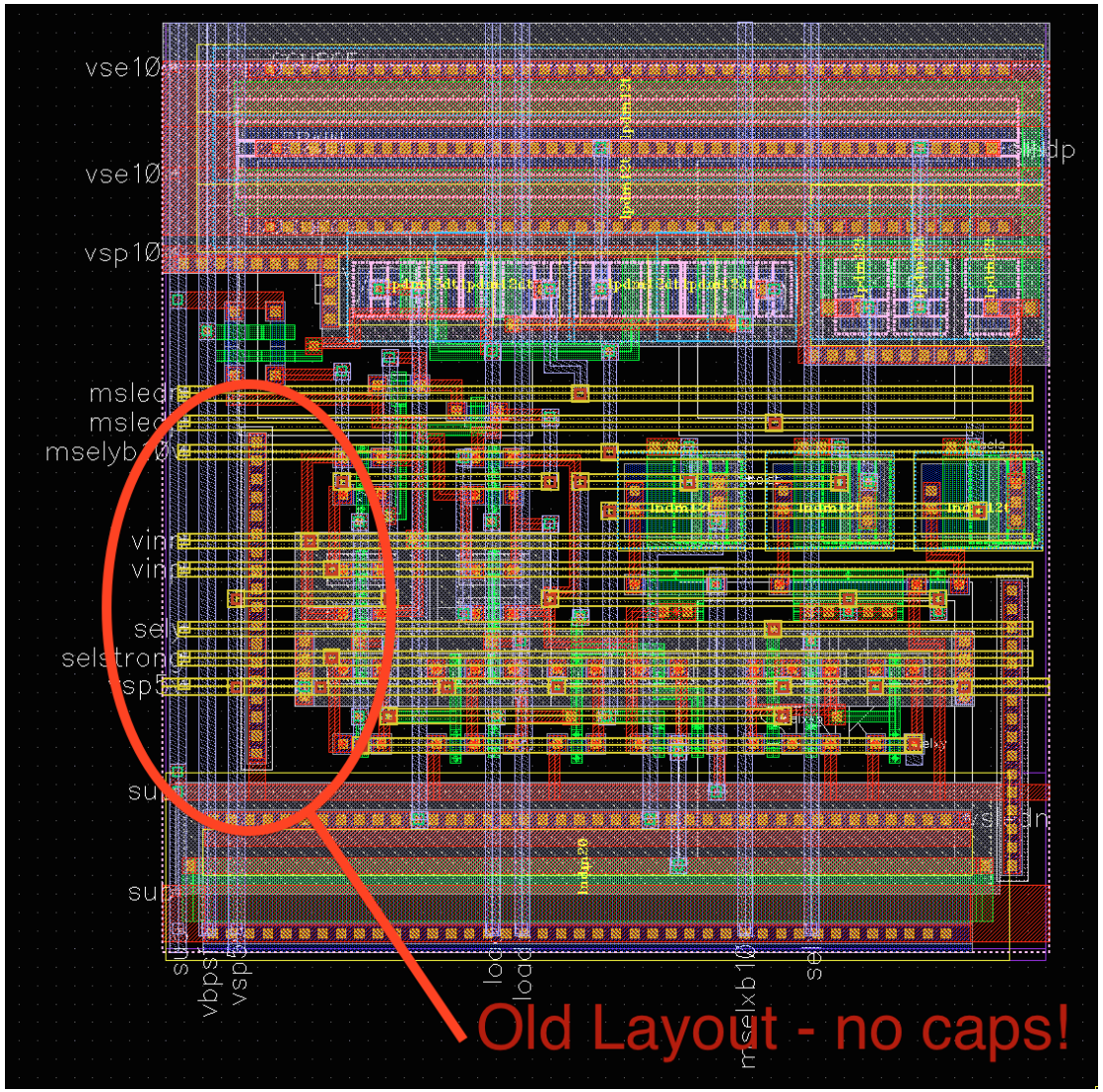
- Two color LEDs
- Snap Shot mode
- Drive strength control



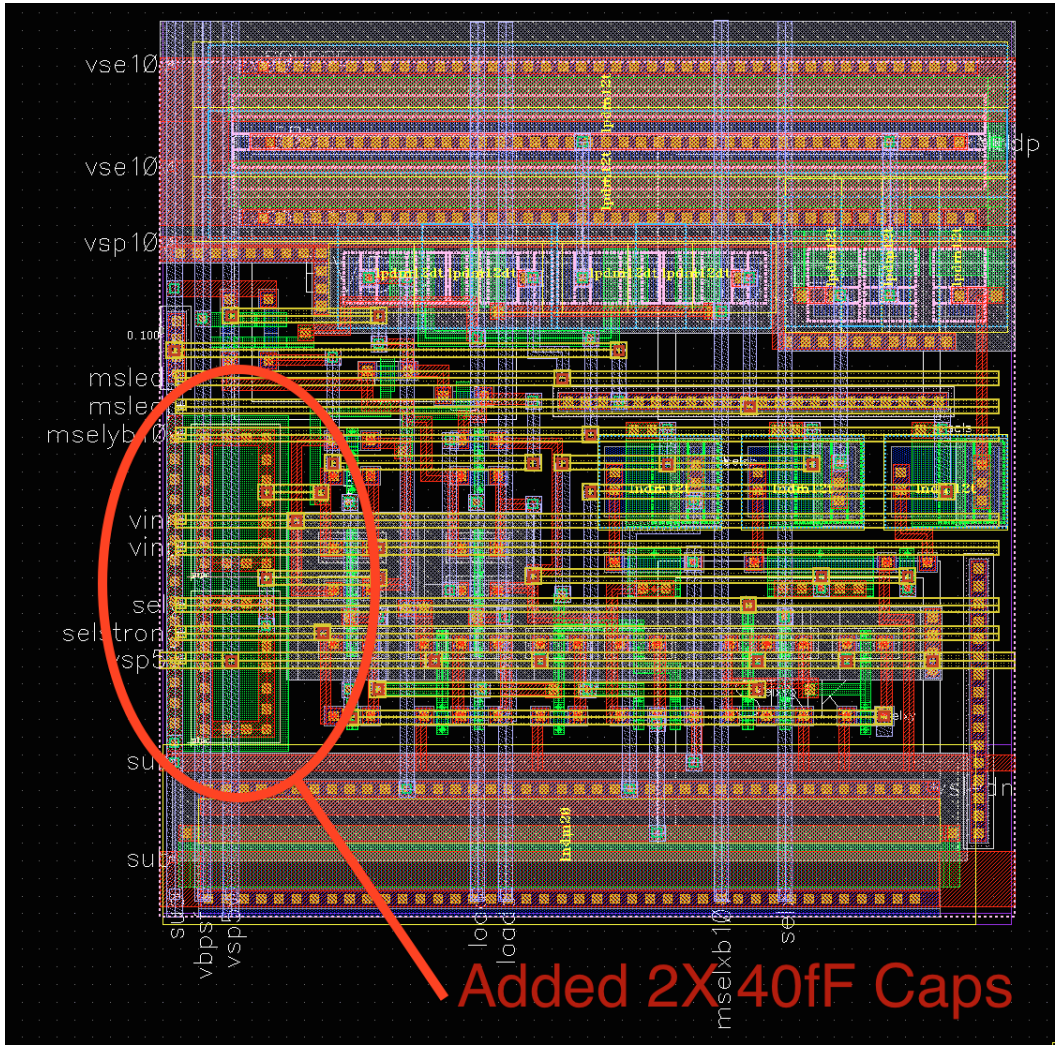


vinp
vinn
selstrong
selx
sely
vsp5v
vsp10v
vse10v
sub
load
loadb
vbpsfn
mselxb10v
mselyb10v
vsledp
vsledn
msledp
msledn

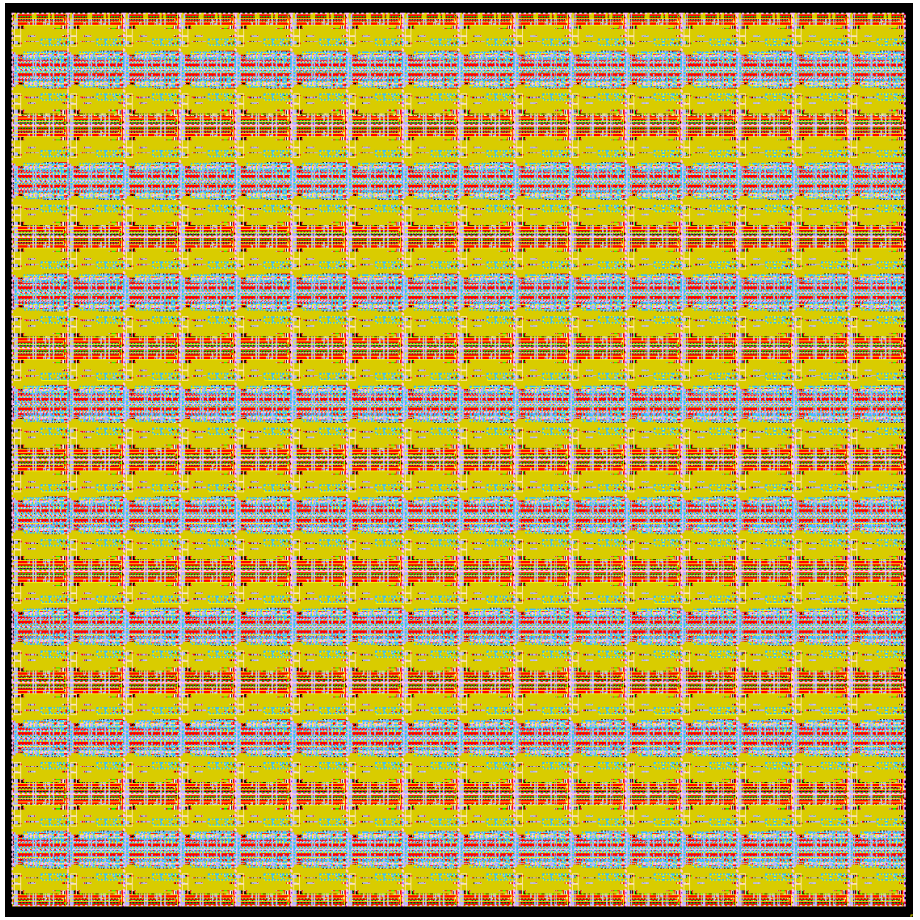
Two Color CMOS Pixel



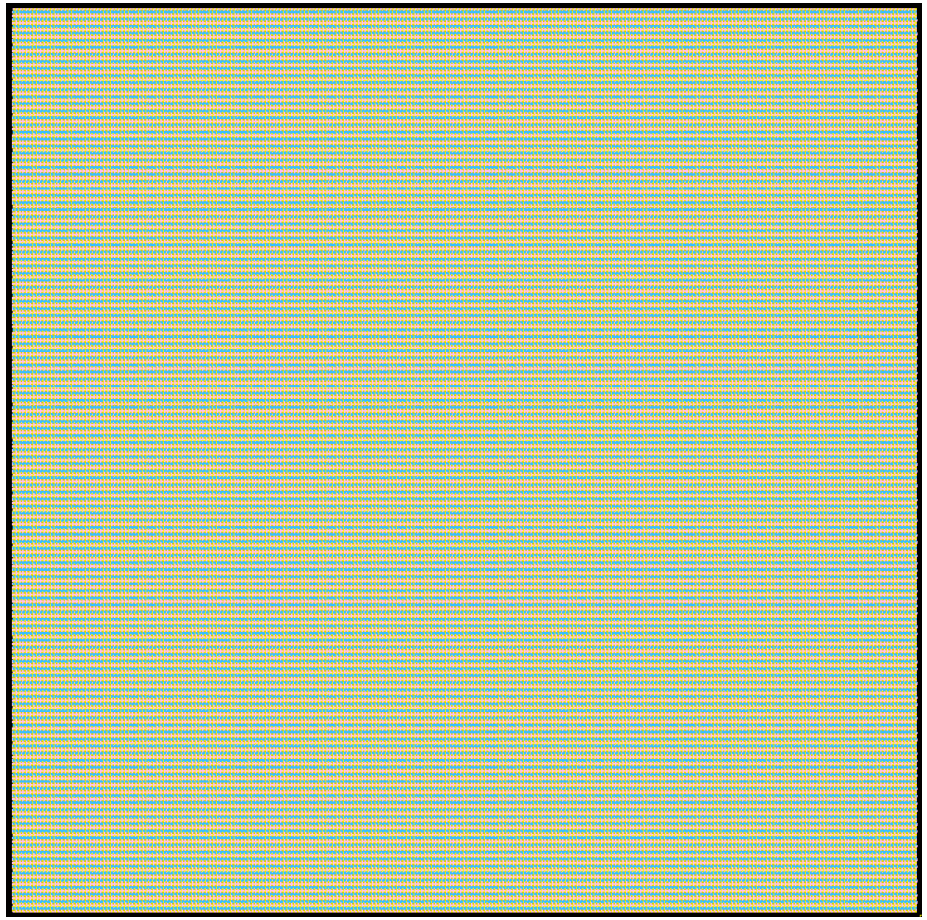
Two Color CMOS Pixel With Analog Memory



Pixel Array Zoomed Out



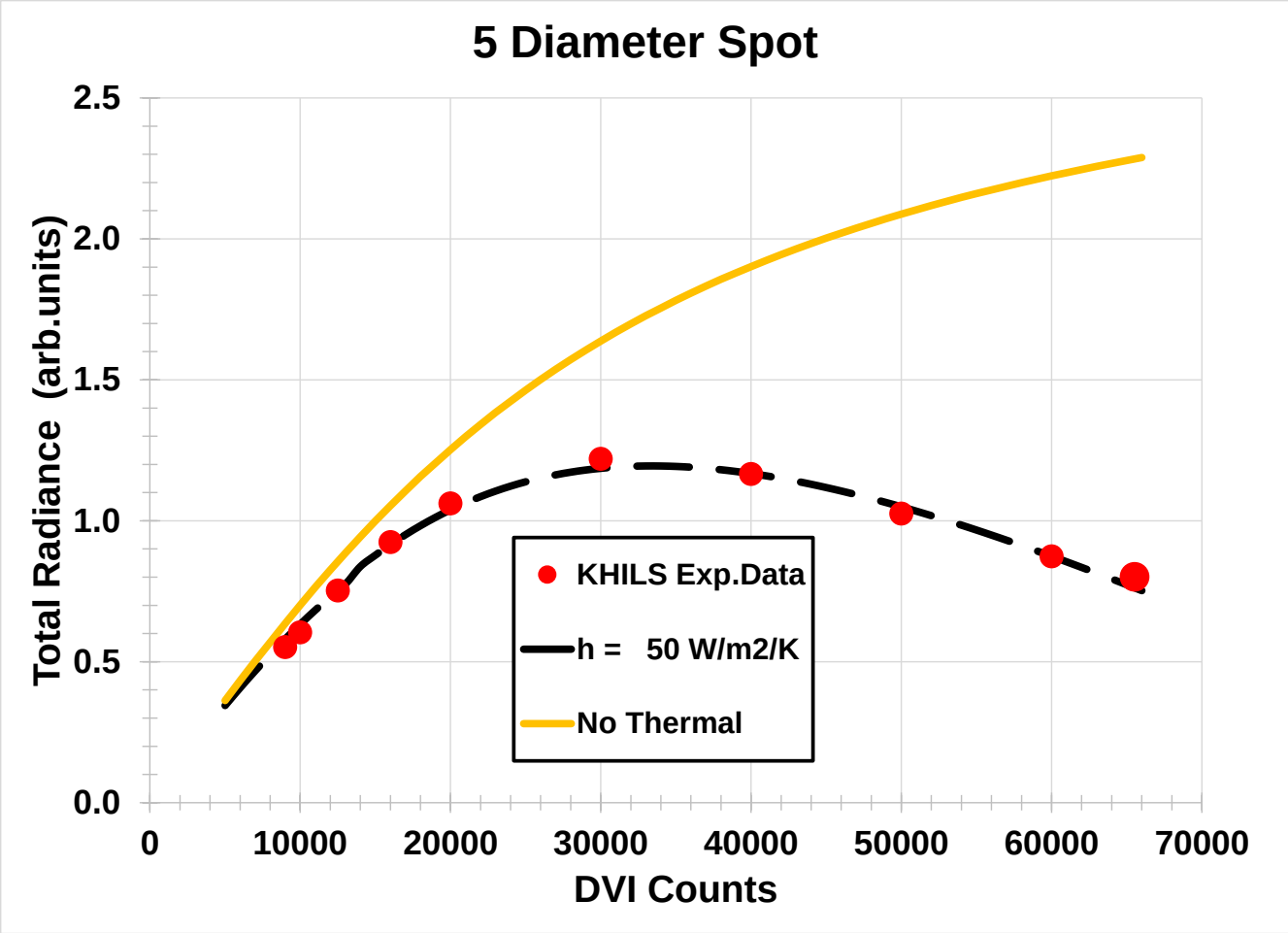
Pixel Array Even More Zoomed Out

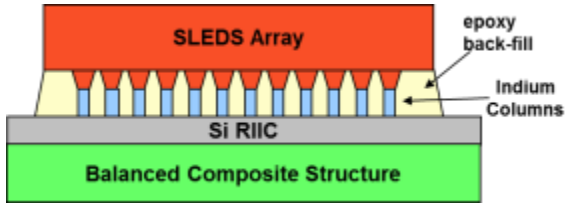


Power Considerations

- Each pixel in a SLED array at full power dissipates 12 volts and 15 milliamps.
- If all pixels in a 512 by 512 array were turned on, the array would dissipate 47 kW!

Thermal Problems for Performance





Current Bonded Composite Substrate (BCS) Structure

2 mil GaSb SLEDs array =>

5 micron indium posts with epoxy =>

10 mil silicon CMOS RIIC =>

1.5 mil epoxy with dielectric spheres =>

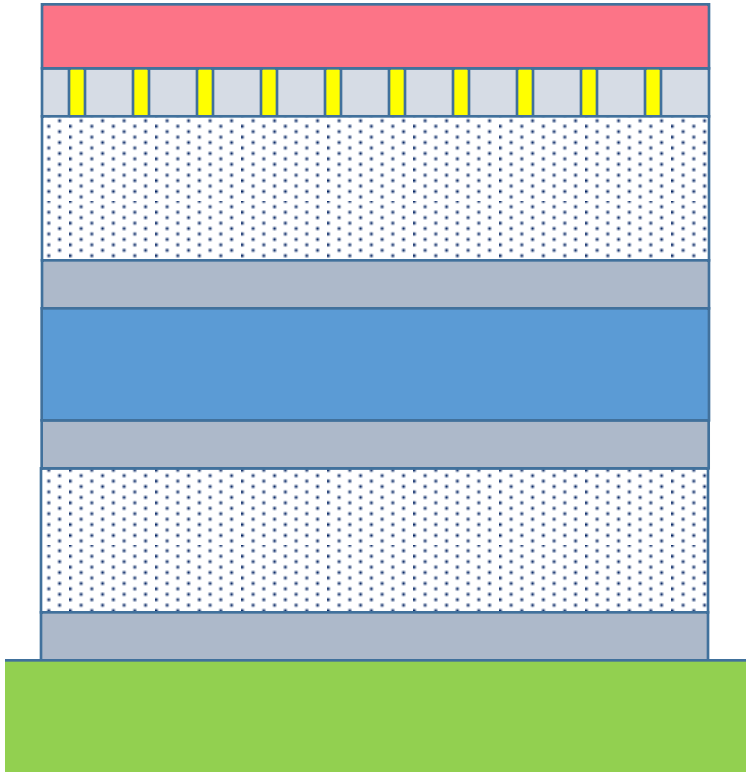
5 mil stressor =>

1.5 mil epoxy with dielectric spheres =>

10 mil silicon wafer =>

1.5 mil epoxy with dielectric spheres =>

Heat sink =>



Thermal Conductivities	
Material	**Thermal Cond. [W / m*K]**
Silicon	130
GaSb	32
Indium	82
Molebdenum	138
Unfilled Epoxy	0.15
Filled Epoxy	1 to 1.4

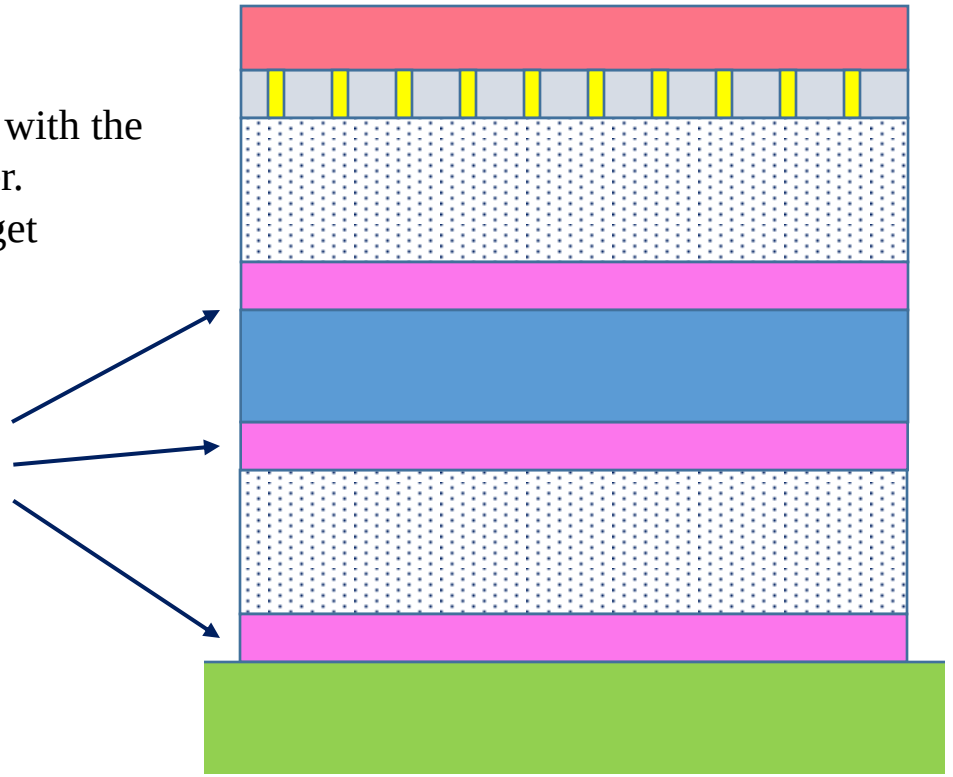
Semiconductor Thermal Conductivities from http://www.ioffe.rssi.ru/SVA/NSM/Semicond/index.html

Use a High Thermal Conductivity Epoxy

- BN filled epoxy can have a thermal conductivity in the 1 to 1.4 W/mK. [1]

- Requires heavy loading of the epoxy with the high thermal conductivity filler.
- Careful epoxy dispense needed to get a thin void-free glue line.

High thermal conductivity epoxy



1- 3M TC-2810 BN filled epoxy- http://solutions.3m.com/wps/portal/3M/en_US/Electronics_NA/Electronics/Products/Product_Catalog/~/3M-Thermally-Conductive-Epoxy-Adhesive-TC-2810?N=4294286417+5153906&&Nr=AND%28hrcy_id%3A6VHXX34PP0gs_NB1DMCTNL4_N2RL3FHWVK_GPD0K8BC31gv%29&rt=d

Eliminate Two of the Three Epoxy Joints

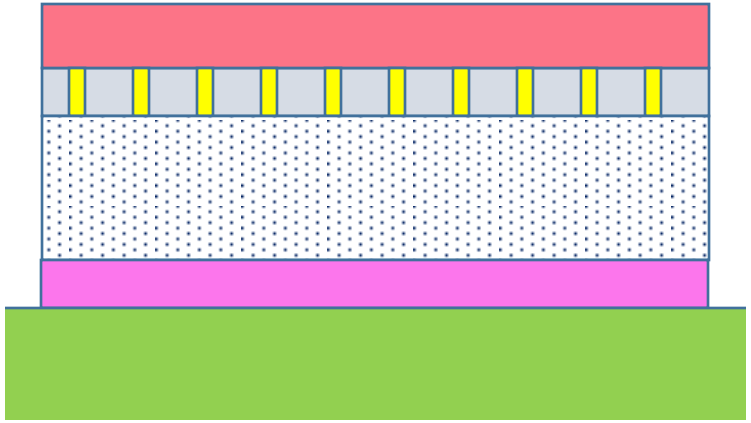
2 mil GaSb SLEDs array =>

5 micron indium posts with epoxy =>

10 mil silicon CMOS RIIC =>

High thermal conductivity epoxy =>

Metal heat sink =>



Coefficient of thermal expansion of GaSb = 7.75 e-6 $^{O}C^{-1}$

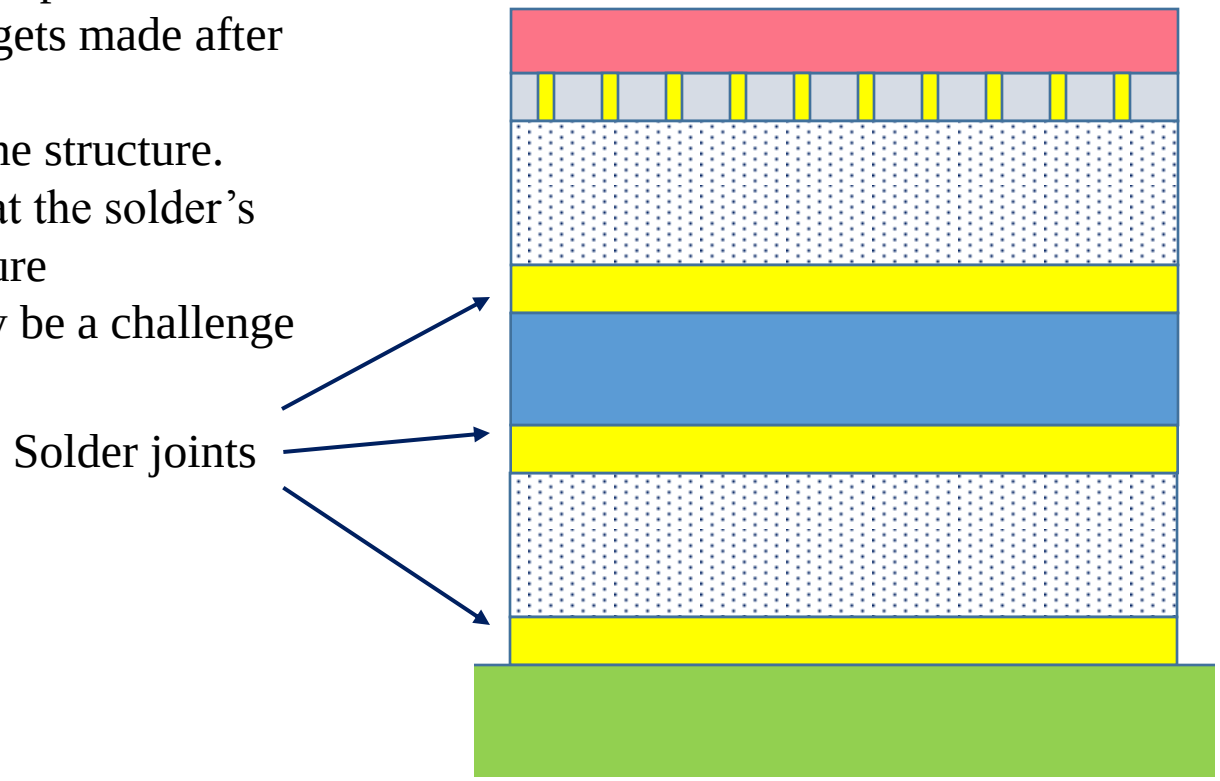
- In cooling a one cm square GaSb chip from 300K to 80K results in the chip getting 17 um smaller.

Coefficient of thermal expansion of silicon= 2.6 e-6 $^{O}C^{-1}$

Coefficient of thermal expansion of molybdenum = 5 e-6 $^{O}C^{-1}$

Replace the Epoxy Joints with a Solder Joints

- Two soldering steps are needed.
  - BCS joints “need” to be done at the wafer level, before indium bumps are fabricated.
  - Bottom solder joint gets made after hybridization.
- Builds more stress into the structure.
  - Layers lock together at the solder’s freezing temperature
- Maintaining flatness may be a challenge



Reflow Method CTE Stack Up

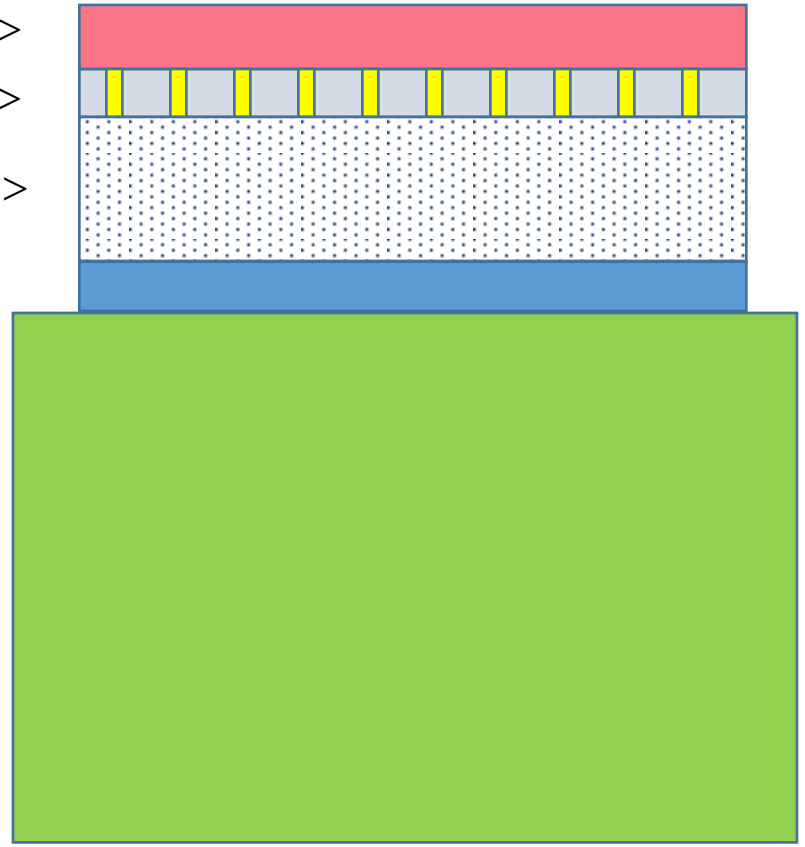
CTE

2 mil GaSb SLEDs array => $7.75 \cdot 10^{-6}\ °C^{-1}$

5 micron indium posts with epoxy => $29 \cdot 10^{-6}\ °C^{-1}$

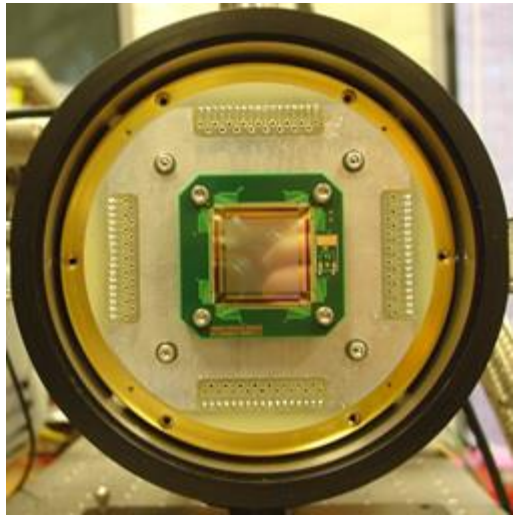
10 mil silicon CMOS RIIC => $2.6 \cdot 10^{-6} °C^{-1}$

Solder =>

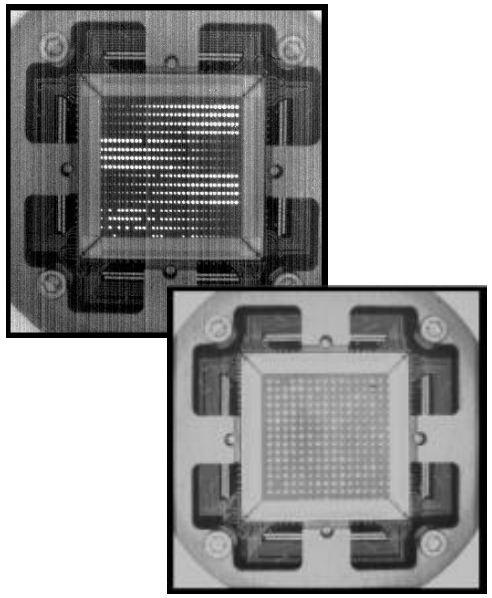


Thermal Block CuW => $7.2 \cdot 10^{-6}\ °C^{-1}$

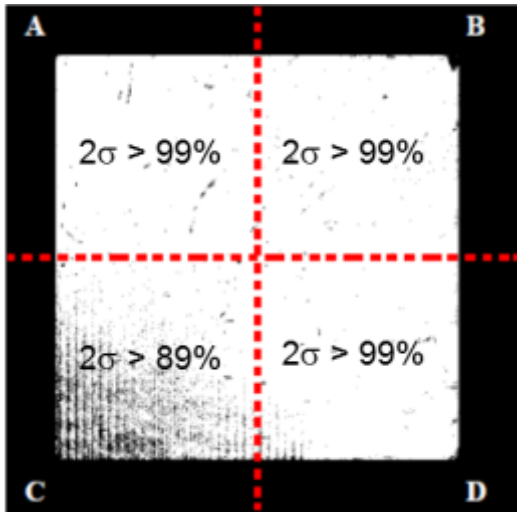
SLEDS Phase 2 Efforts



512x512 SLEDS Mounted In Dewar



Sparse Grid Patterns



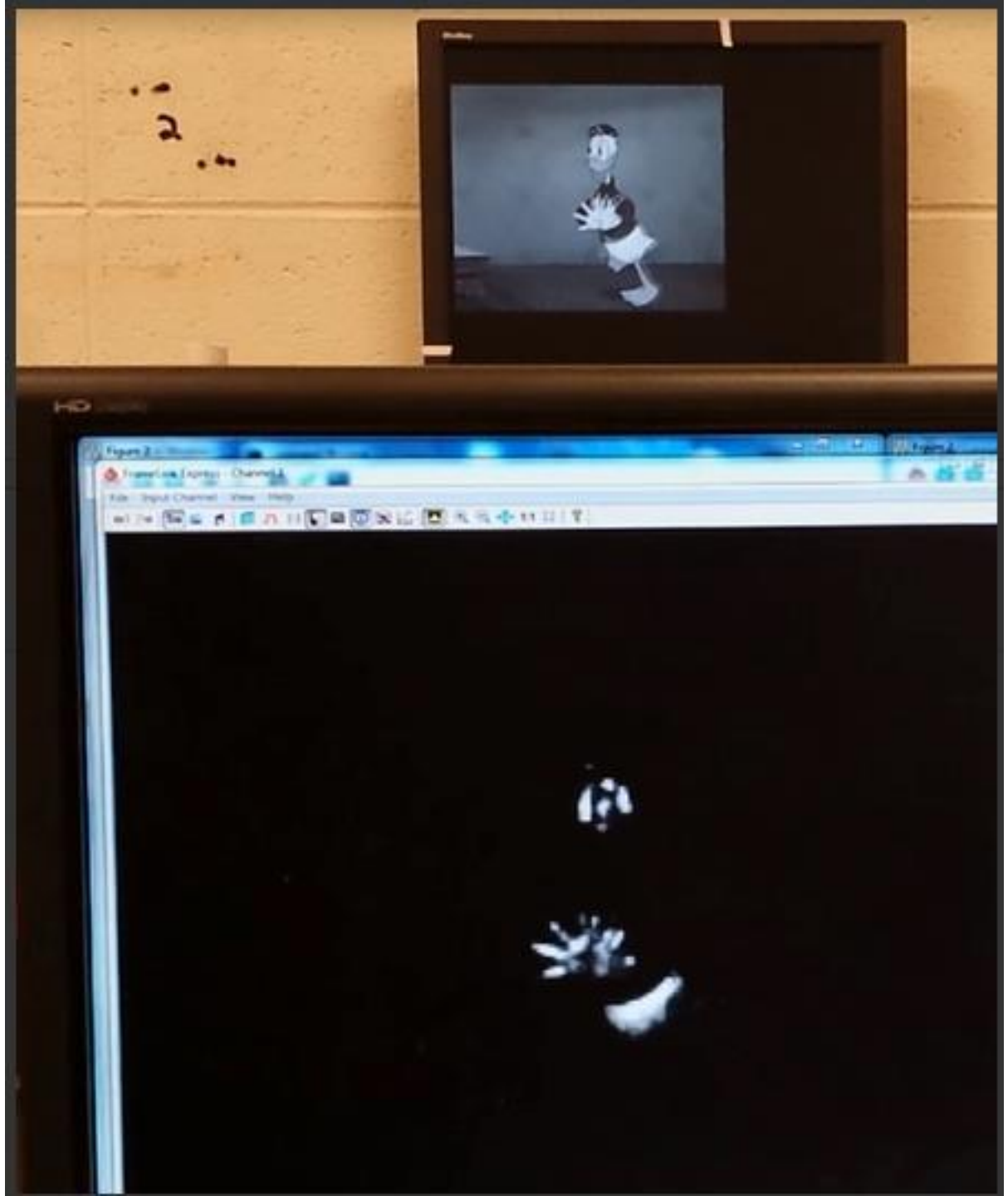
Operability Map

- **First demonstration of a hybridized 512x512 MWIR LED array**
- **Three quadrants with > 99% operability; one with > 89% operability - etching nonuniformity, which has been corrected**
- **Identified modest CSE electronics improvements to reach 100Hz**
- **Identified CSE and RIIC improvements to reach 1KHz**

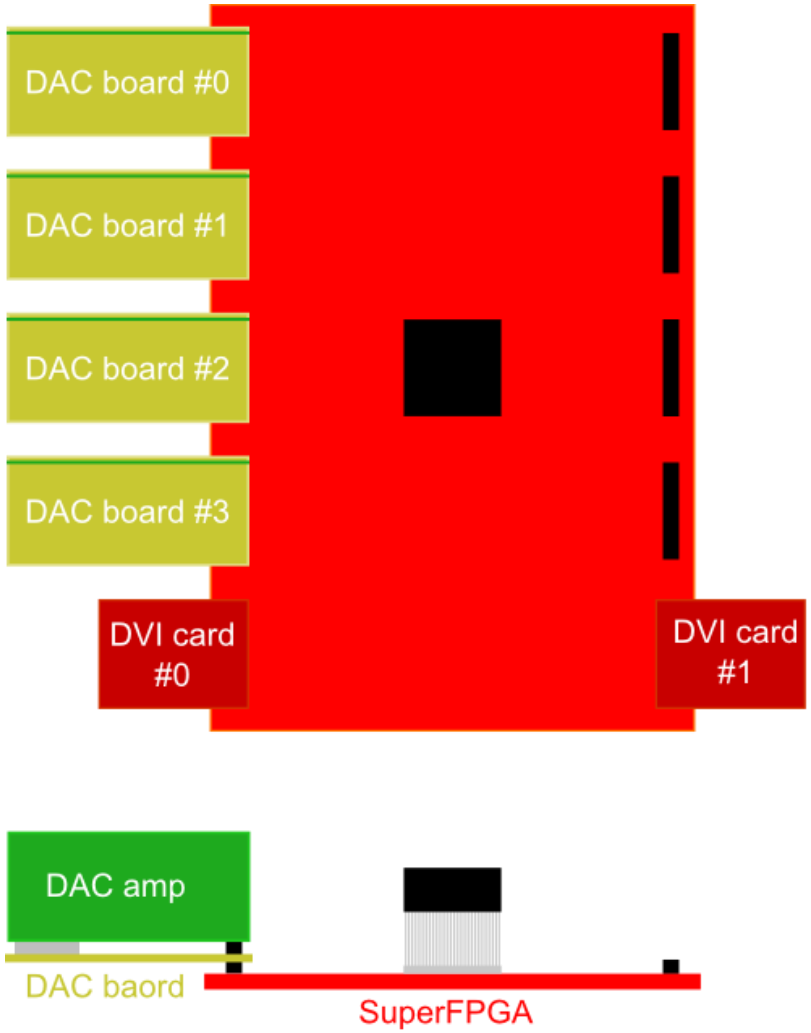
SLEDs Projector

SLEDS Projector

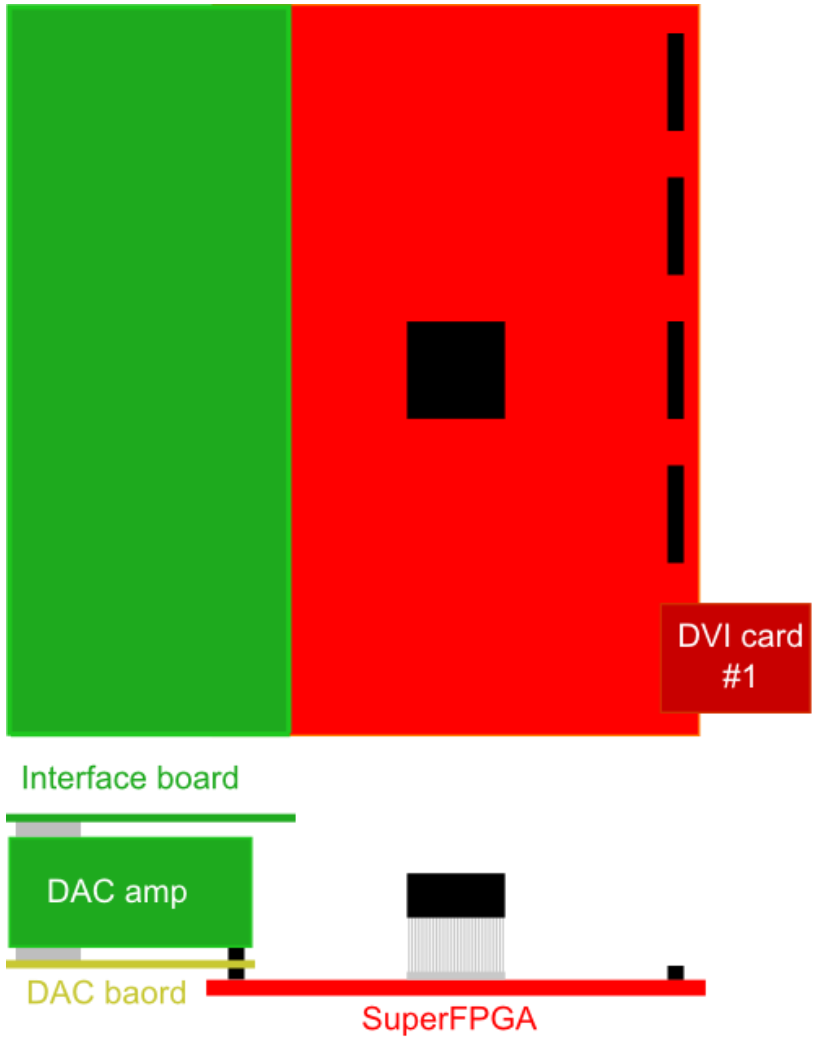
- Single color
- Original pixel circuit
- Notice the inability to draw light spots



Close Support Electronics

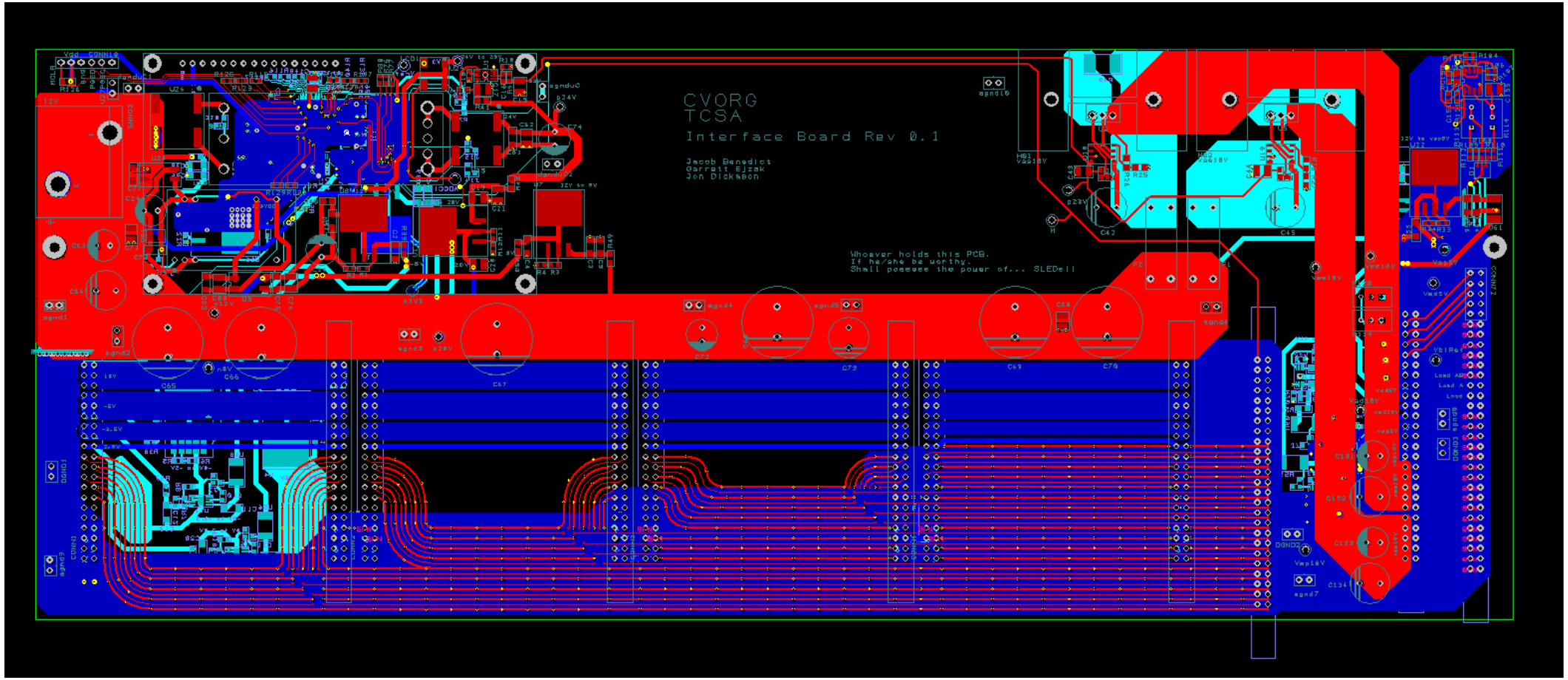


Four DAC without Interface

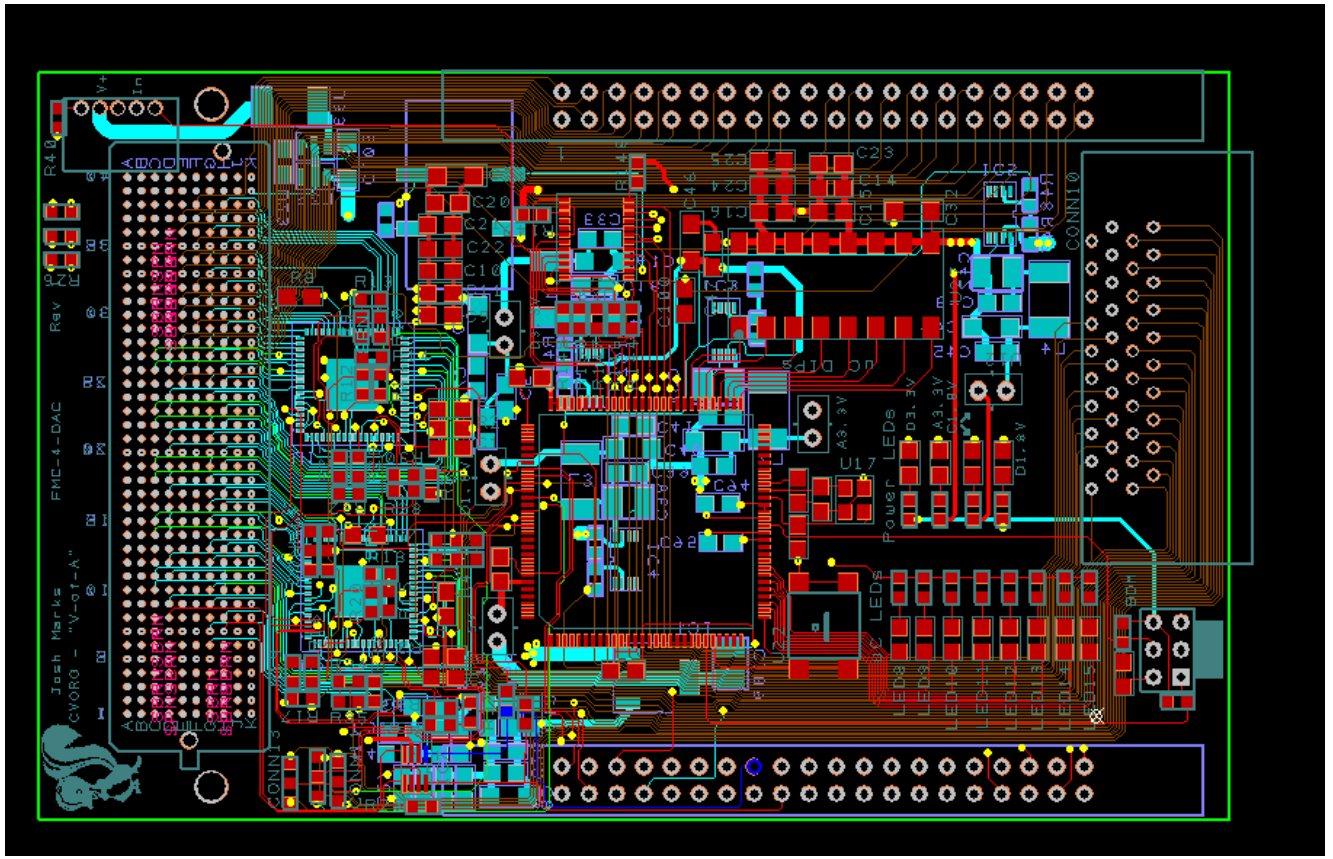


Four DAC with Interface

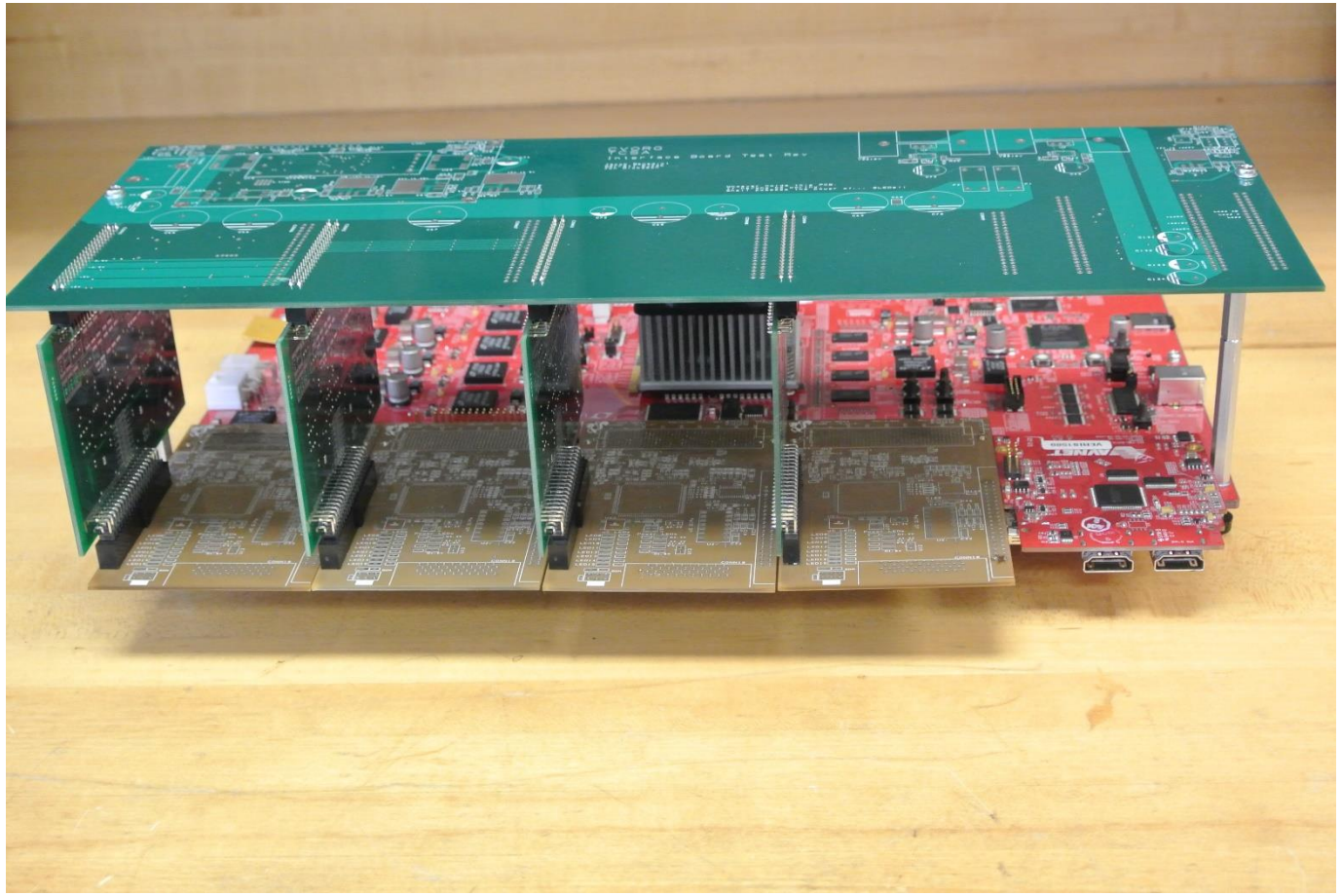
Interface Board Layout



DAC Board Layout



Close Support Electronics



Close Support Electronics