Toward Extreme-Scale High-Performance Computing Using a Fine-Grain Dataflow-Inspired Execution Model

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Outline

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   - The Von Neumann Model
   - The Dataflow Model
3. **The Codelet Model: Harnessing Parallelism in Shared-Memory Multi/Many Core Systems**
4. **DARTS: An Implementation of the Codelet Model**
   - DARTS: Implementation of the Codelet Machine Model
   - DARTS: Experimental Results
     - Running DGEMM in DARTS
     - Running Graph500 in DARTS
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   - The TERAFLUX Project
   - Porting DARTS to COTSon
   - DARTS/COTSon: Experimental Results
6. **The Future of Codelets**

2004–2005: Apparition of Multi-Core Systems

- The power wall leads to the first multi-core processors
- Memory wall: a major performance issue (See Wulf and McKee 1995)
- GPUs become more programmable (but still through dirty hacks)

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- Intel proposes "real" multi-core processors (but still use a front-side bus)
- AMD provides an efficient interconnect for NUMA architectures
- IBM unveils the POWER6, Cell B.E. and Cyclops-64
- Nvidia uncovers CUDA (No need to resort to dirty hacks anymore)

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2008–2010: Toward “Many-Core” Compute Nodes

- Compute nodes start to propose a large number of cores
  - *e.g.*, 8-Core Intel Nehalem EX: 4×16 threads per node, with a NUMA Interconnect
- Nvidia commercializes boards dedicated to supercomputing

Meanwhile, in Versailles. . .

- 2006: Compiler transformation – Deep Jam
- 2007–2008: Methodology to fine-tune kernels on multicore systems
- 2009–2010: A balanced approach to application performance tuning
- 2010: Tackling cache line stealing in multicore systems

See Carribault et al. 2007; Zuckerman, Pérache, and Jalby 2008; Koliaï et al. 2009; Risio et al. 2009; Charif Rubial et al. 2009; Zuckerman and Jalby 2010

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Main Parallel Programming Models

- MPI
- OpenMP
- CUDA

...for adventurers only

What to Expect for the Next Generation HPC Systems?

- Core/thread count per processor is rising
- Amount of cache per core/thread is decreasing
- Memory is becoming a *severe* bottleneck
  - Many people think coherence will have to go

Parallel Programming in 2005–2010

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How will we program the next parallel processors?

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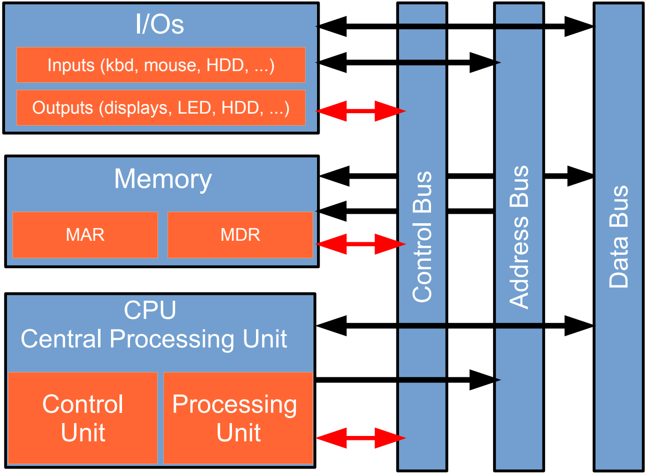
A Short Introduction to Execution Models

The von Neumann Model – a High-Level View



Advantages of the von Neumann Model

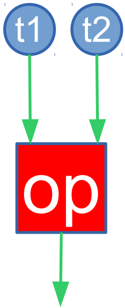
- Simple
- Can almost be implemented "directly"
  - However nobody would design a processor this way nowadays

Limitations of the von Neumann Model

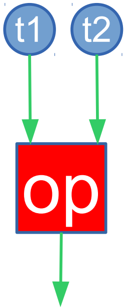
- Relies on a *sequence* of instructions
- Time is thus an integral part of the model
- Makes use of an accumulator: side-effects are inherent to the model
  - Reduces the potential for parallelism

Working Around Those Limitations

- Duplicate several "von Neumann machines," each with their own PC
- Add buses to share both memory and I/Os between processors
- . . . Is it still a von Neumann machine then?



t1
t2
op

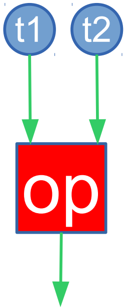


Static Dataflow Actors

Components of a regular actor:

- Input arcs which may contain at most 1 token each
- Output arcs which may contain at most 1 token each
- The operation provided by the actor
- Tokens

See Dennis, Fosseen, and Linderman 1972; Dennis 1974; Dennis and Misunas 1974



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Firing Rule: Static Dataflow

An actor may *fire* when:

- All of its input arcs contain a token, and
- Its output arcs are empty.

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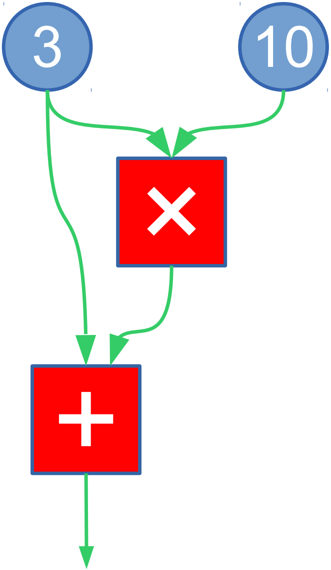
An Example of Dataflow Program



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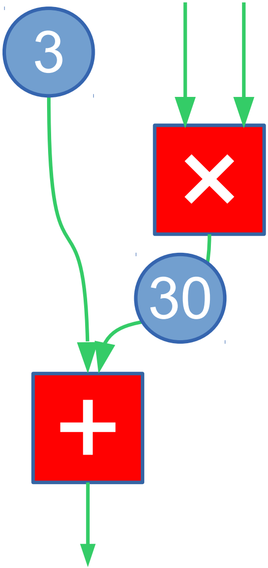

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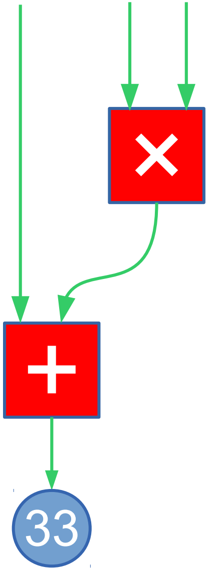


A Short Introduction to Execution Models

The Architecture Model of Static Dataflow

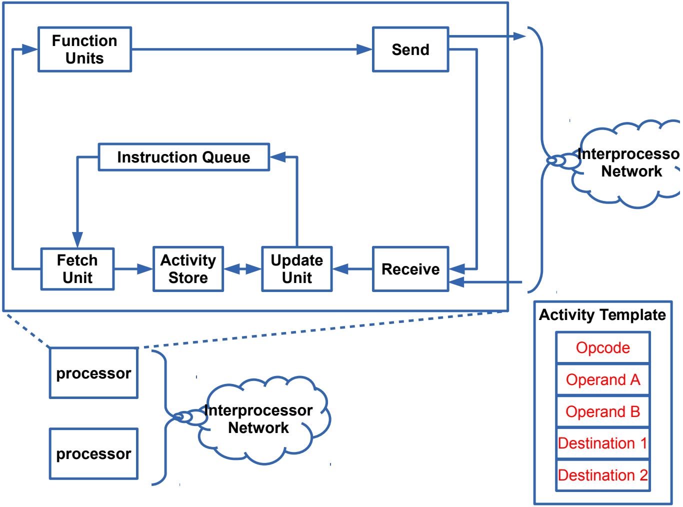
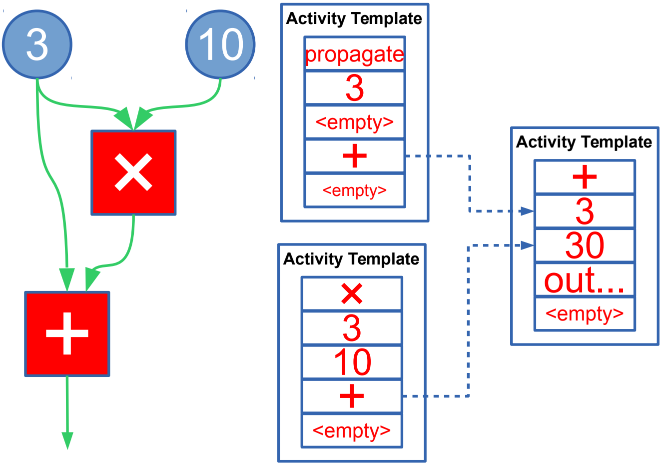


Figure : Inspired by J.Dennis' article (Encyclopedia of Parallel Computing)

Applying Our Example on the Static-DF Arch.



Outline

The Codelet Model: Harnessing Parallelism in Shared-Memory Multi/Many Core Systems

Objectives

- Fine-grain parallelism
- Scalable
- Expose maximal parallelism
- Limits non-determinism (determinate-by-default)
- Handles dynamic events (power, resiliency, resource constraints in general)

Definition

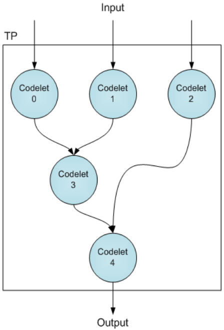
A codelet is a sequence of machine instructions which act as an atomically-scheduled unit of computation.

See DARPA-BAA-10-37 2010-2012; Carter et al. 2013; Department of Energy 2012–2014

The Codelet Model: Harnessing Parallelism in Shared-Memory Multi/Many Core Systems

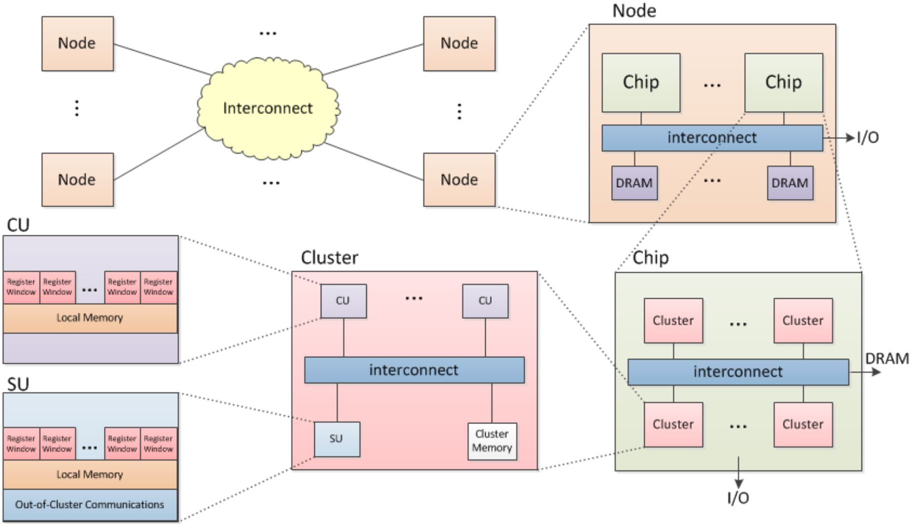
Properties

- Event-driven (availability of data and resources)
- Communicates only through its inputs and outputs
- Non-preemptive (with very *specific* exceptions)
- Requires all data and code to be “local”



See Zuckerman, Suetterlein, et al. 2011

The Codelet Abstract Machine



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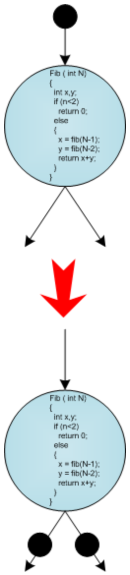
Codelet Graphs: Operational Semantics

Codelet Firing Rule

- Codelet actors are *enabled* once tokens are on each input arc
- Codelet actors fire by
  - consuming tokens
  - performing the operations within the codelet
  - producing a token on each of its output arcs

States of a Codelet

- Dormant: Not all tokens are available
- Enabled: All *data* tokens are available
- Ready: All tokens are available
- Active: The codelet is executing internal operations



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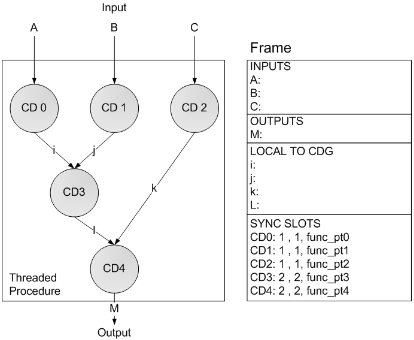
TPs are containers for codelet graphs, with additional meta-data.

Description

- Invoked in a control-flow manner
- Called by a codelet from another CDG
- Feature a frame which contains the context of the CDG



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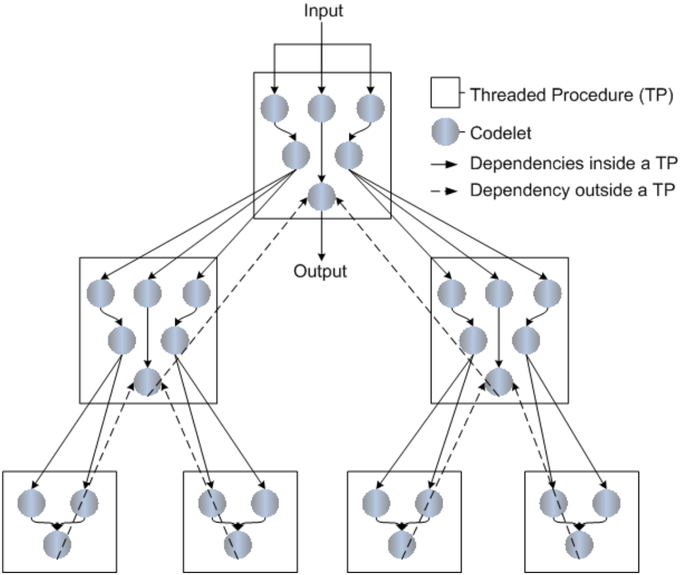
An Example of Computation Using Threaded Procedures



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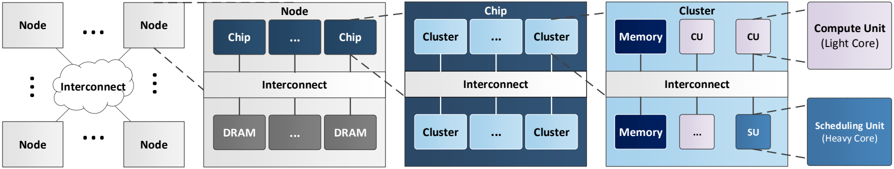
Objectives

- Faithfulness to the codelet execution model
- Modularity
  - So that portions of the runtime can be added or changed easily
  - For example: we have several codelet schedulers from which to choose
- Portability: Object-oriented, written in C++98, and makes use of open-source libraries:
  - `hwloc`: to determine the topology of the underlying system (HW threads/cores, caches, *etc.*)
  - If present on the system, it uses Intel TBB's lock-free queues

See Suetterlein, Zuckerman, and Gao 2013

DARTS: Implementation of the Codelet Machine Model

- Computation Units (CUs) embed a single producer/consumer ring buffer to store ready codelets
- Synchronization Units (SUs) embed two pools: Threaded Procedures and ready codelets.
- Heavy reliance on lock-free data structures
- SUs can temporarily assume the role of CUs if all other CUs are busy and there are ready codelets left to execute.



See Suetterlein, Zuckerman, and Gao 2013

Experimental Setup

AMD Opteron 6234 (Bulldozer) – Mills – 128 GiB DDR DRAM

		Cache Level	Shared By	Size (KiB)
Clock (GHz)	2.4	L1 Data	1 core	16
Threads / core	1	L1 Instruction	1 core	64
Cores / socket	12	L2 Unified	2 cores	2048
Sockets / node	4	L3 Unified	6 cores	6144
Compiler		gcc v4.6		
Math Library		AMD Core Math Library (ACML) v5.3		

Note: FPUs are shared between 2 cores.

Intel Xeon E5-2670 (Sandy Bridge) – FatNode – 64 GiB DDR3 DRAM

		Cache Level	Shared By	Size (KiB)
Clock (GHz)	2.6	L1 Data	2 threads	32
Threads / core	2	L1 Instruction	2 threads	32
Cores / socket	8	L2 Unified	2 threads	256
Sockets / node	2	L3 Unified	8 threads	20480
Compiler		gcc v4.7		
Math Library		Intel Math Kernel Library (MKL) v11.1		

Note: Functional units are shared between 2 threads.

Running DGEMM in DARTS – Codelet Graph

Description of DGEMM

- **D**ouble precision **GE**neral **M**atrix **M**ultiplication
- Used ACML or MKL as sequential building blocks (no tiling/blocking, *etc.*, needed)
- We compared several codelet scheduling policies within a cluster of cores

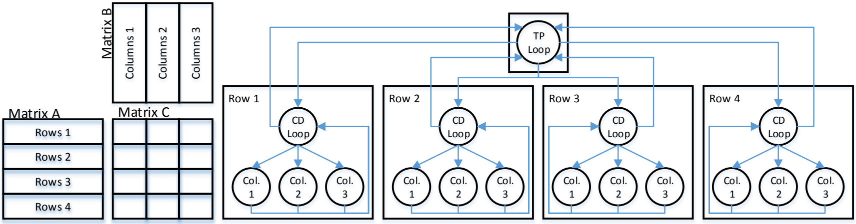


Figure : Our Codelet Graph decomposition for a parallel DGEMM

See Suetterlein, Zuckerman, and Gao 2013

Running DGEMM in DARTS – Mills – Strong Scaling

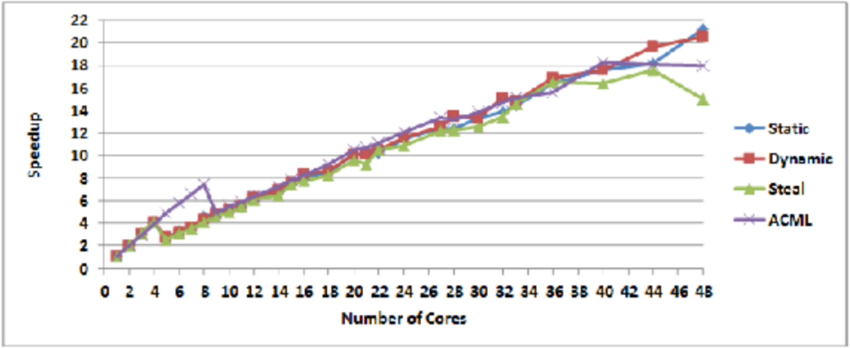


Figure : 10000×10000 Square DGEMM – Strong Scaling.

See Suetterlein, Zuckerman, and Gao 2013

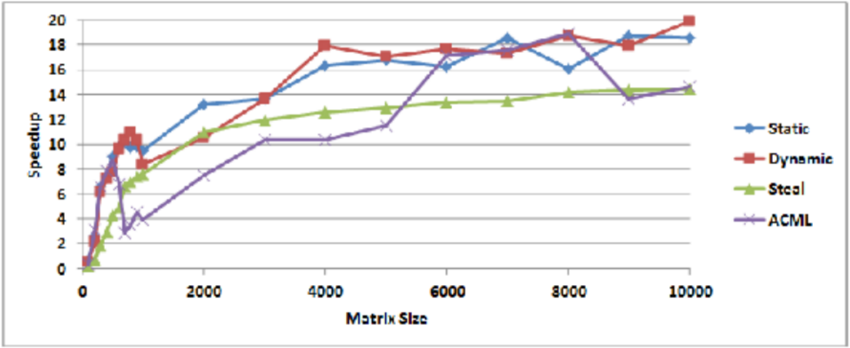


Figure : 48 cores – Square DGEMM – Weak Scaling.

See Suetterlein, Zuckerman, and Gao 2013

Running DGEMM in DARTS – FatNode – Strong Scaling

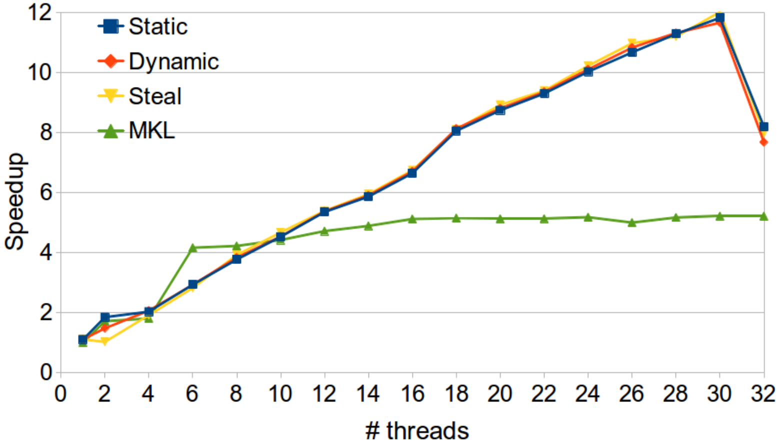


Figure : 3072×3072 Square DGEMM – Strong Scaling.

Running DGEMM in DARTS – FatNode – Weak Scaling

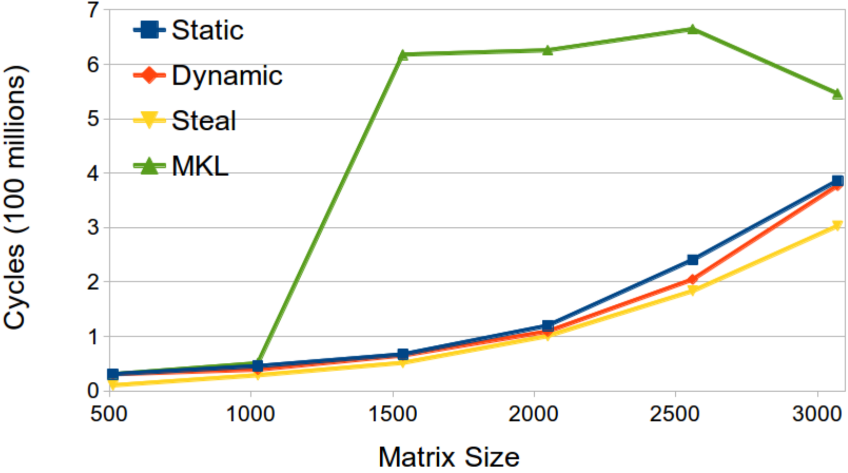
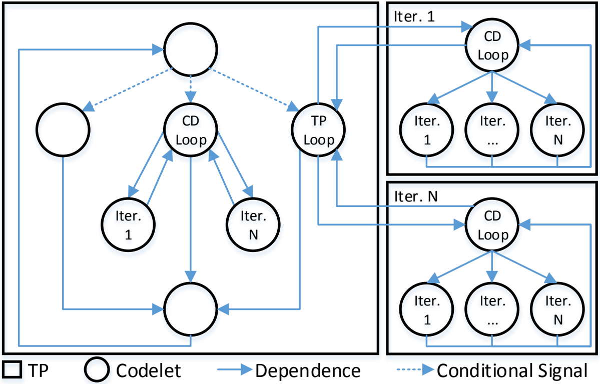


Figure : 32 threads – Square DGEMM – Weak Scaling.

Running Graph500 in DARTS – Codelet Graph

Description of Graph500

- Reused reference code (`http://graph500.org`)
- Only modified the breadth-first search phase (BFS)
- Compared with reference OpenMP parallelization
- Unit: Traversed Edges Per Second (TEPS)



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Running Graph500 in DARTS – Mills – Strong Scaling

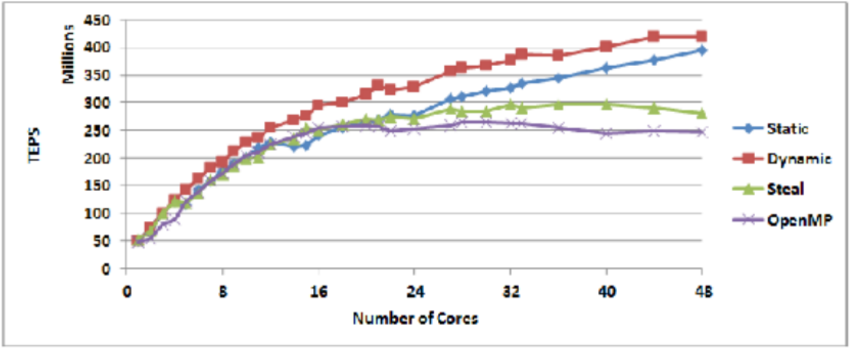
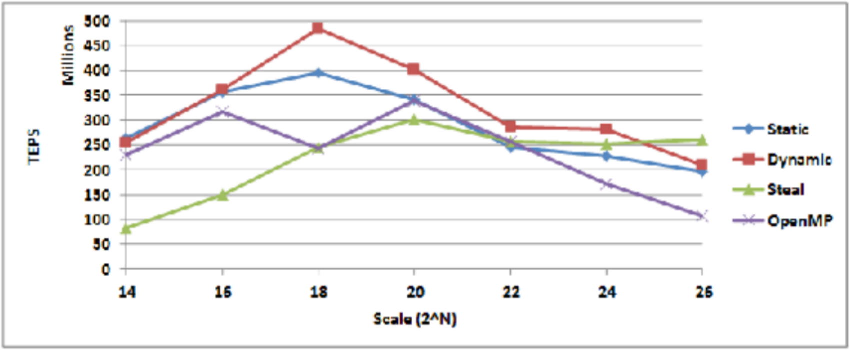


Figure : $Scale = 2^{18}$ – Graph500 – Strong Scaling

See Suetterlein, Zuckerman, and Gao 2013

Running Graph500 in DARTS – Mills – Weak Scaling



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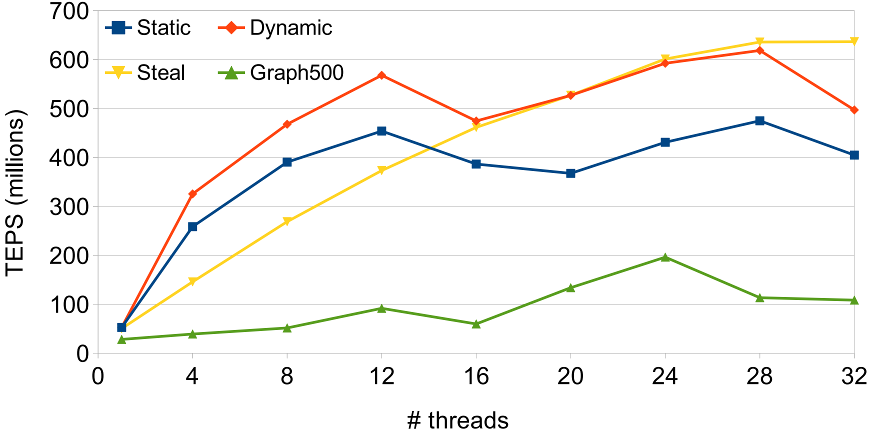

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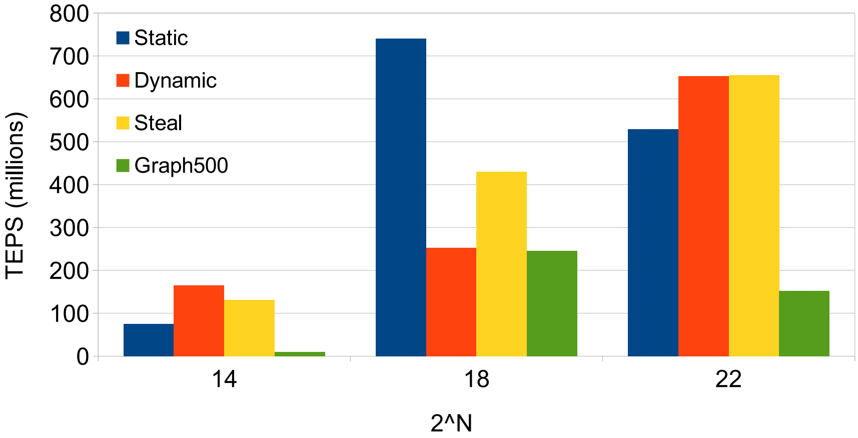

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Project Objectives

Future Teradevice systems will expose a large amount of parallelism (1000+ cores) that cannot be exploited efficiently by current applications and programming models. The aim of this project is to propose a complete solution that is able to harness the large-scale parallelism in an efficient way. The main objectives of the project are the programming model, compiler analysis, and a scalable, reliable, architecture based mostly on commodity components. Data-flow principles are exploited at all levels as to overcome the current limitations.

For more details, see `http://teraflux.eu`

See Solinas et al. 2013; Giorgi et al. 2014; Zuckerman, Arteaga, et al. 2014

The DF-Thread Model

- A *DataFlow Thread* (DF-Thread) is a non-preemptive piece of code which is ready to be *fired* when all its data dependencies are met.
- A DF-Frame contains all the data required by the DF-Thread to run.
  - While there are dependencies left, a DF-Frame is write-only
  - Once all dependencies are met, the frame becomes read-only
- The TERAFLUX abstract machine model features:
  - A Thread Scheduling Unit (equivalent of the Codelet Model's SU)
  - A Fault-Detection Unit (to handle fault-tolerance)

See Solinas et al. 2013; Giorgi et al. 2014; Zuckerman, Arteaga, et al. 2014

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See Solinas et al. 2013; Giorgi et al. 2014; Zuckerman, Arteaga, et al. 2014

- Two key differences:
  - 1 level of parallelism (DF-Threads) vs. 2 (Codelets + TPs)
  - Each DF-Thread has its own private frame
  - All codelets belonging to a TP share the same TP frame (and data)
- DARTS maps each codelet to a DF-Thread, with a minimal DF-frame
- The TP frame shared by codelets siblings is allocated on the heap
- All codelets belonging to a TP are constrained to the same node

See Solinas et al. 2013; Giorgi et al. 2014; Zuckerman, Arteaga, et al. 2014

- Adding a codelet to the graph during execution triggers the call to `df_tschedule(&Fire,nb_deps,sizeof(Codelet*))`
- The `Fire` function is tasked to call the `Codelet::fire()` function and then clean up after using `df_destroy()`
- Threaded procedures are called using the `invoke<ThdProc>(parameters)` function:
  - Parameters are marshalled along with the TP type, and bundled within a DF-Thread
  - When firing, the DF-Thread allocates the TP on the heap, along with all of its codelets

See Solinas et al. 2013; Giorgi et al. 2014; Zuckerman, Arteaga, et al. 2014

All latencies were obtained using CACTI. We used COTSon's dynamic samplers to measure time (sample = 5M instructions).

	Private / Shared	Size	Number of Sets	Cache Line Size (Bytes)	Latency
L1D cache	private	16 KiB	4	64	2
L1I cache	private	32 KiB	4	64	2
L2U cache	private	64 KiB	4	64	5
L3U cache	shared	4 MiB	8	128	10

See Solinas et al. 2013; Giorgi et al. 2014; Zuckerman, Arteaga, et al. 2014

Running Fibonacci in DARTS – TERAFLUX

Strong Scaling

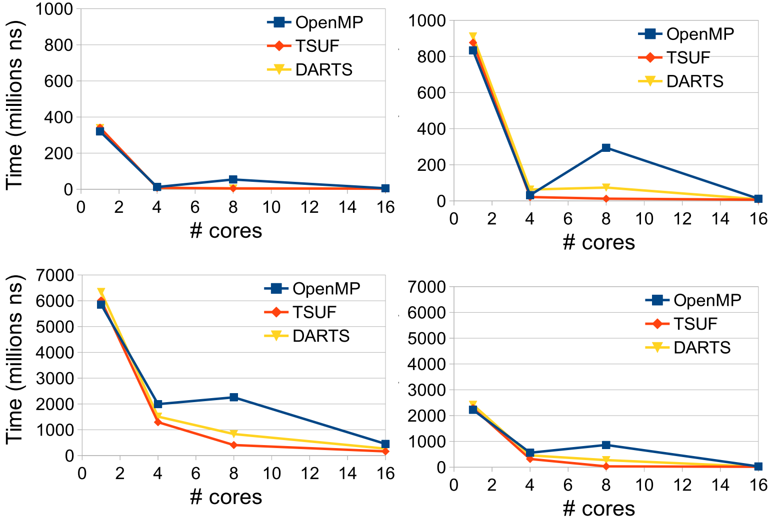


Figure : *Cutoff* $= 18$ – Fibonacci – $n = 36$ – Strong Scaling

Running Fibonacci in DARTS – TERAFLUX

Weak Scaling

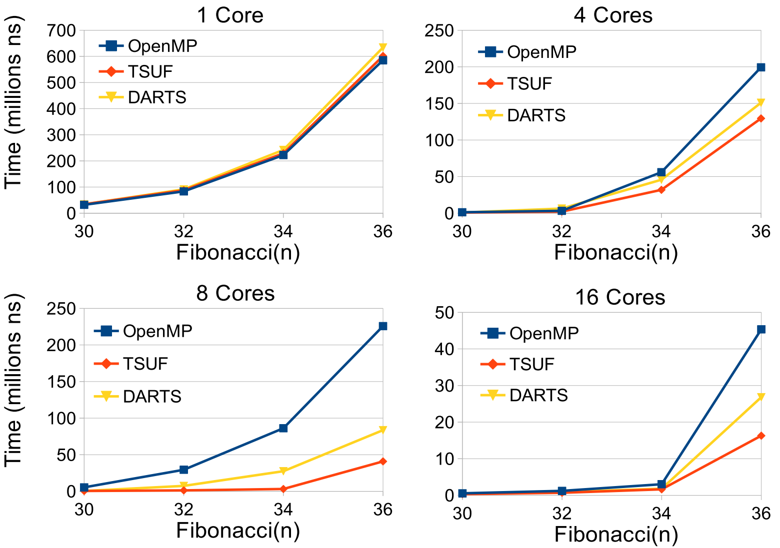


Figure : $Cutoff = 18$ – Fibonacci(n) – Weak Scaling

Running Merge Sort in DARTS – TERAFLUX

Strong Scaling

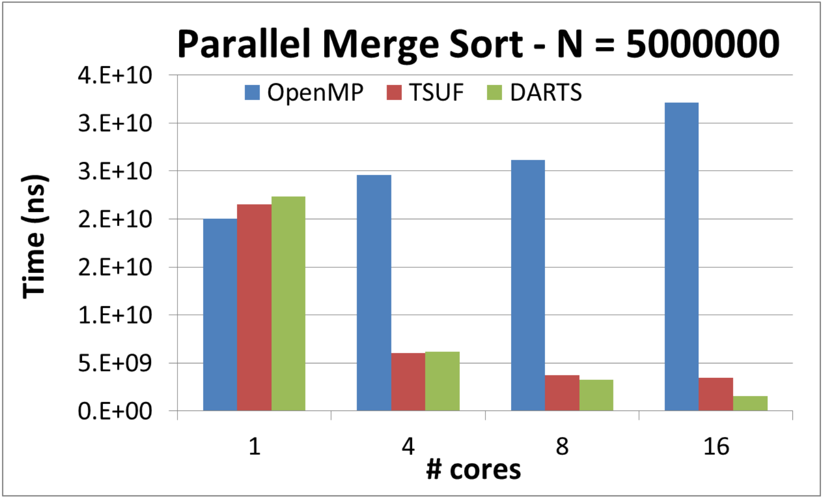


Figure : *Cutoff* $= 18$ – Merge Sort – $n = 5M$ elements – Strong Scaling

Running Merge Sort in DARTS – TERAFLUX

Weak Scaling

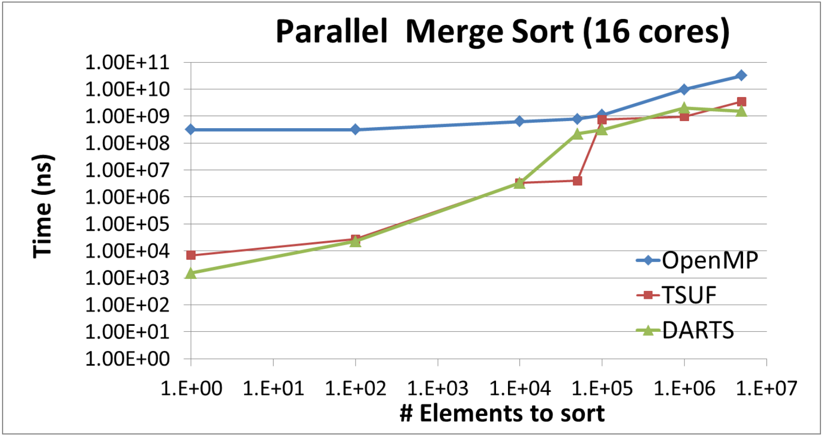


Figure : *Cutoff* = 10000 – Merge Sort(n) – Weak Scaling

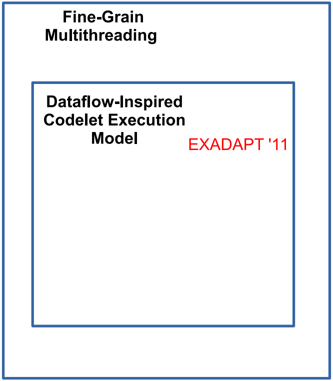
See Zuckerman, Arteaga, et al. 2014

Outline

The Future of Codelets

The Story So Far

- We proposed the codelet execution model to answer the need for scalability, performance, energy efficiency, fault-tolerance, and programmability
- Experimental results show that the Codelet Model can be competitive with current multicore environments
- With hardware support, the Codelet Model displays very high potential to scale to large numbers of cores



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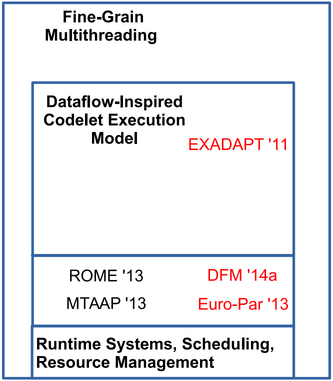

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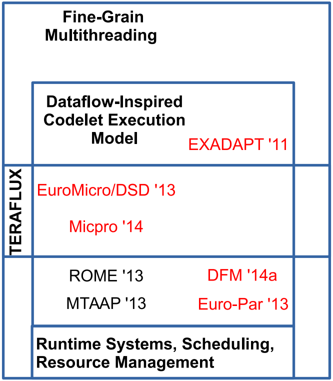
- With hardware support, the Codelet Model displays very high potential to scale to large numbers of cores



The Future of Codelets
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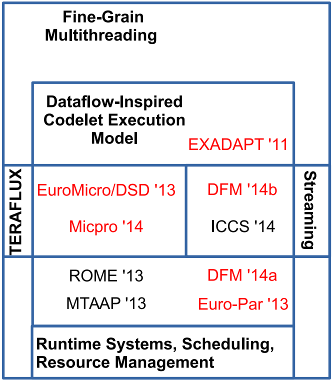

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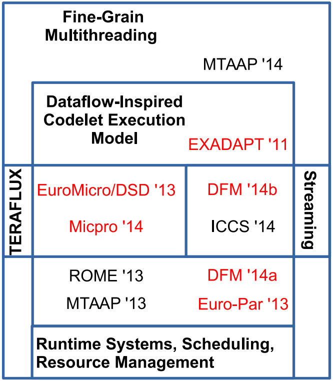
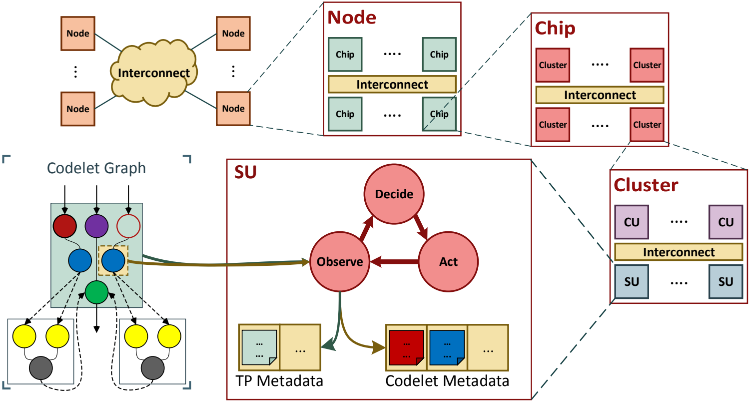


Extending the Codelet Model

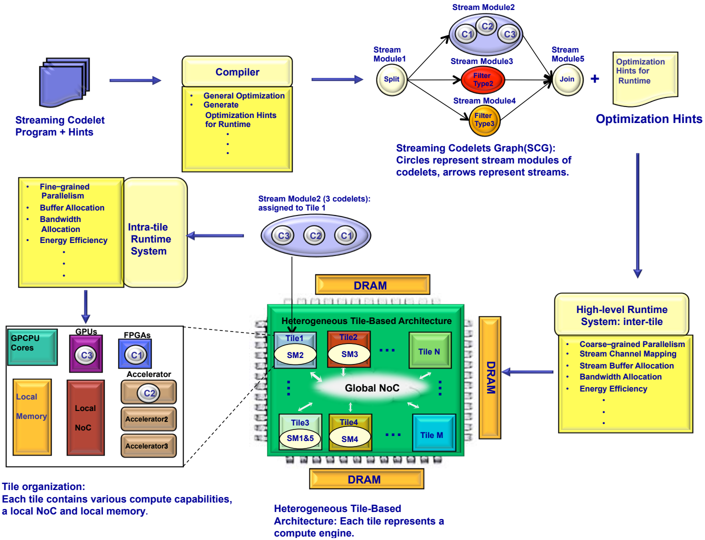
Extending Codelets to Self-Awareness



See Zuckerman, Landwehr, et al. 2014 for more details.

Extending the Codelet Model

Extending Codelets to Streams



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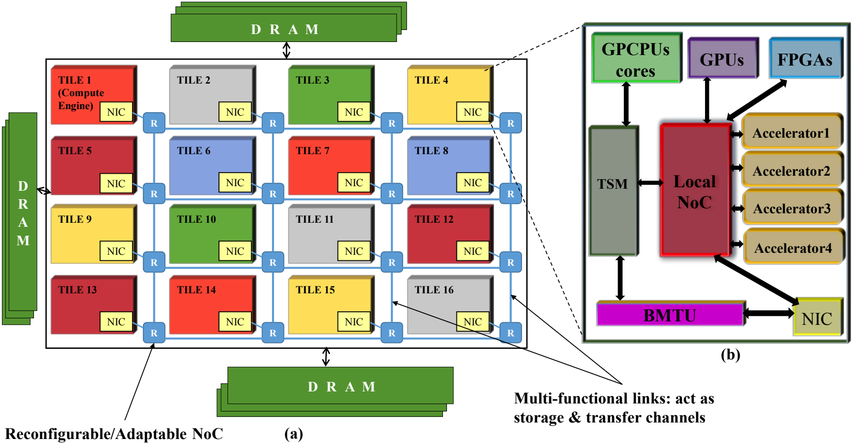

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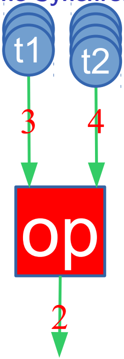
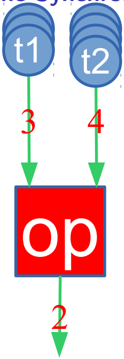
Past and present CAPSL members,

Brian	Lucas	Jaime	Arteaga
Joseph	Manzano	Chen	Chen
Daniel	Orozco	Elkin	Garcia
Robert	Pavel	Souad	Koliaï
Sergio	Pino	Aaron	Landwehr
Jürgen	Ributzka	Josh	Landwehr
Sunil	Shrestha	Kelly	Livingston
		Joshua	Suetterlein
Pouya	Fotouhi	Haitao	Wei
José	Monsalve	Yao	Wu

. . . And of course, Professor Gao!

The Synchronous Dataflow Model (Lee and Messerschmitt 1987)





Synchronous Dataflow Actors

Components of a regular actor:

- Input arcs; each input arc i_l can contain a certain number $k_l i$ of tokens
- Output arcs; each output arc o'_l can contain a certain number $k'_{l'}$ of tokens
- The operation provided by the actor
- Tokens

A Short Introduction to Execution Models

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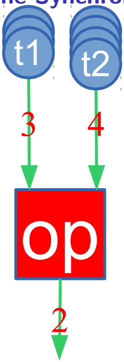

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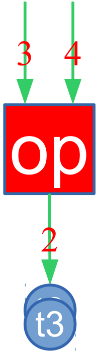
Firing Rule: Synchronous Dataflow (SDF)

An actor may *fire* when:

- Each of its input arcs in the tuple $< i_0, i_1, \cdots, i_{k-1} >$ contains at least $< n_0, n_1, \cdots, n_{k-1} >$ tokens, and
- The number of slots available on each of the output arcs $< o_1, o_2, \cdots, o_{k'-1} >$ is sufficient to receive an additional count of n' tokens.



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Other Dataflow Models

Dynamic Dataflow

- Allows for arbitrary recursions
- Relies on “color-matching:”
  - Each iteration is assigned a “color,”
  - An actor only fires if all tokens from the same color are present on its input arcs.
- Proved to provide maximum parallelism
- However: Color matching is *slow* (use of hash tables, . . .)

Macro-Dataflow

- Idea: Instead of relying on fine-grain, one-operation-at-a-time actors, let’s use a bunch of instructions/operations in sequence within the actor
- Still relies on inputs and outputs, but now the buffers may become much bigger, due to the amount of work and data required
- Offers a compromise to reduce the signaling overhead of fine-grain dataflow, token matching, *etc.*

See Watson and Gurd 1982; Arvind and Culler 1986; Papadopoulos and Culler 1990; Arvind and Gostelow 1982

Extending the Codelet Model

Extending Codelets to Self-Awareness

Future extreme-scale systems will most likely feature thousands of cores on a chip, and deep memory hierarchies. The Codelet Model was created with this in mind. However several problems still need to be tackled:

- Memory movements are expected to cost much more than computations in terms of energy consumption
- There will be a need for fine-grain resource management to target goals such as:
  - Maximum or average power envelope during computation required by the user
  - Degree of parallelism in the application declared by the user
  - Maximum acceptable temperature levels
  - ...
- We want to augment codelets and threaded procedures with meta-data which describe their resource usage
- A low-level runtime will then be able to make smart decisions based on static meta-data as well as updated data collected during the codelets executions
- The runtime will then be able to decide when to turn on/off parts of the manycore ships, when to rely on DVFS techniques, *etc.*

See Zuckerman, Landwehr, et al. 2014 for more details.

Dataflow naturally maps to streams. However, the *nature* of future extreme-scale manycore processors will most likely be widely different:

- Heterogeneity is already becoming a reality at the chip level
  - AMD released its first Fusion processor (CPU+GPU on the same chip) in 2013
  - Next-generation Intel "co-processors" will be on package with traditional multicore chips
  - Nvidia just recently produced an accelerator board which embed arm processors to deal with more control-heavy workloads
- We predict heterogeneity will be ingrained at a much deeper level in processors
- This is a great opportunity to do research in that direction — and in particular by targeting streams

The NSF just accepted to provide funding to explore this venue. A high-level view of our objectives was recently published. See Zuckerman, Wei, et al. 2014 for more details.

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