Landing Codelets PXM on DARTS

DEMAC - Towards a Hardware/Software Codesign/Evaluation Platform

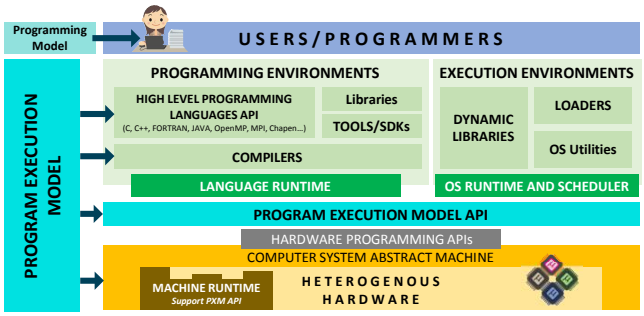
Diego Roa, Jose Monsalve, Ryan Kabrick, Xu Tan, Guang Gao

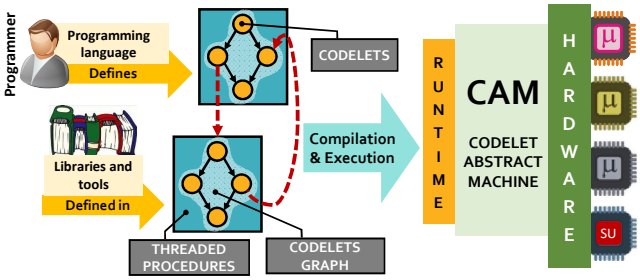
University of Delaware

CAPSL Computer Architecture and Parallel Systems Laboratory

Codeletes (PXM)

Program Execution Models (PXM) define the structure and behavior of a program when executed on an abstract target machine. For parallel systems PXMs describe the program in terms of **synchronization**, **memory models** and **actors** (**tasks**). A common PXM for parallel systems is a key element for the success of parallel programming, as it allows software modularity and portability across multiple systems.

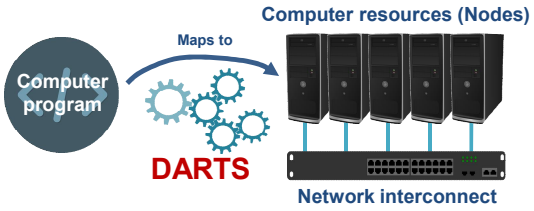


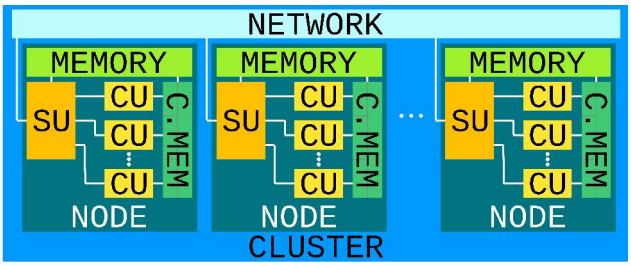


The Codelet model defines a program as a collection of Event and Data driven **tasks**, connected by **Dependencies,** forming a **Codelet Graph (CDG)**. **Threaded Procedures (TPs)** are asynchronous procedures defined by a CDG and its environment and required resources. TP communicate through continuations. Codelets borrow the semantics of Von Neumann PXMs, while CDGs are defined using Dataflow semantics.

DARTS

The Delaware Adaptive Runtime System (DARTS) is an implementation of the Codelet PXM that includes a set of **APIs** and **Compiler Tools** to define **Threaded Procedure** and **Codelets** as well as the mapping of the CAM to the Computer System. A set of libraries define the runtime that implements the behavior of the Codelet PXM.

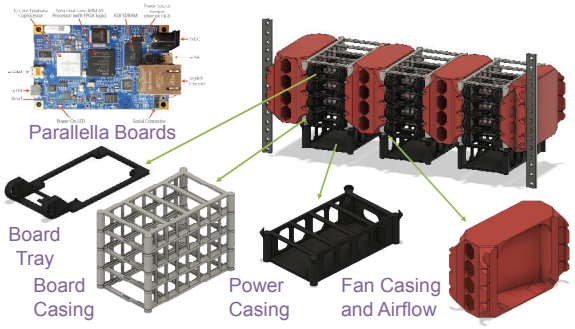


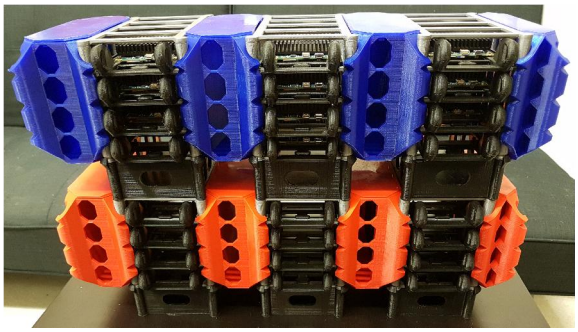


A **Codelet Abstract Machine (CAM)** is used as an abstraction of the underlying hardware. It is made out of **Computational Units** (codelet execution) and **Scheduling Units** (handles resources and synchronization). Memory can be placed at each level of the hierarchy.

DEMAC

The Delaware Modular Assembly Cluster (DEMAC) is an array of Parallella Embedded Systems that combines the many cores Epiphany chip and the embedded FPGA with the flexibility of a complete open source stack. The mount is house made 3D-printed frames allowing low cost implementation and scalability. It is design to fit 4Us of a standard size rack. Files for the rack design are open source. The multiple nodes allows us to explore distributed version of the Codelet Model where there is no notion of shared memory.





Developing hardware level support for the Codelet Model is possible through the use of the FPGA. The many RISC Cores of the Epiphany act as CUs, and the lack of cache coherency, allows us to explore more flexible memory models as well as different mapping mechanisms for the Codelet Abstract Machine. The low cost of the system and its open source promotes interdisciplinary collaborations and expansion of parallel computing to other fields (e.g. Industrial Automation and Robotics)